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INTEGRATED CIRCUIT ELECTROMAGNETIC SUSCEPTIBILITY INVESTIGATION--ETC(U)
JAN 79 J M ROE, J R CHOTT, T W HERRON N60921-76-C-A030
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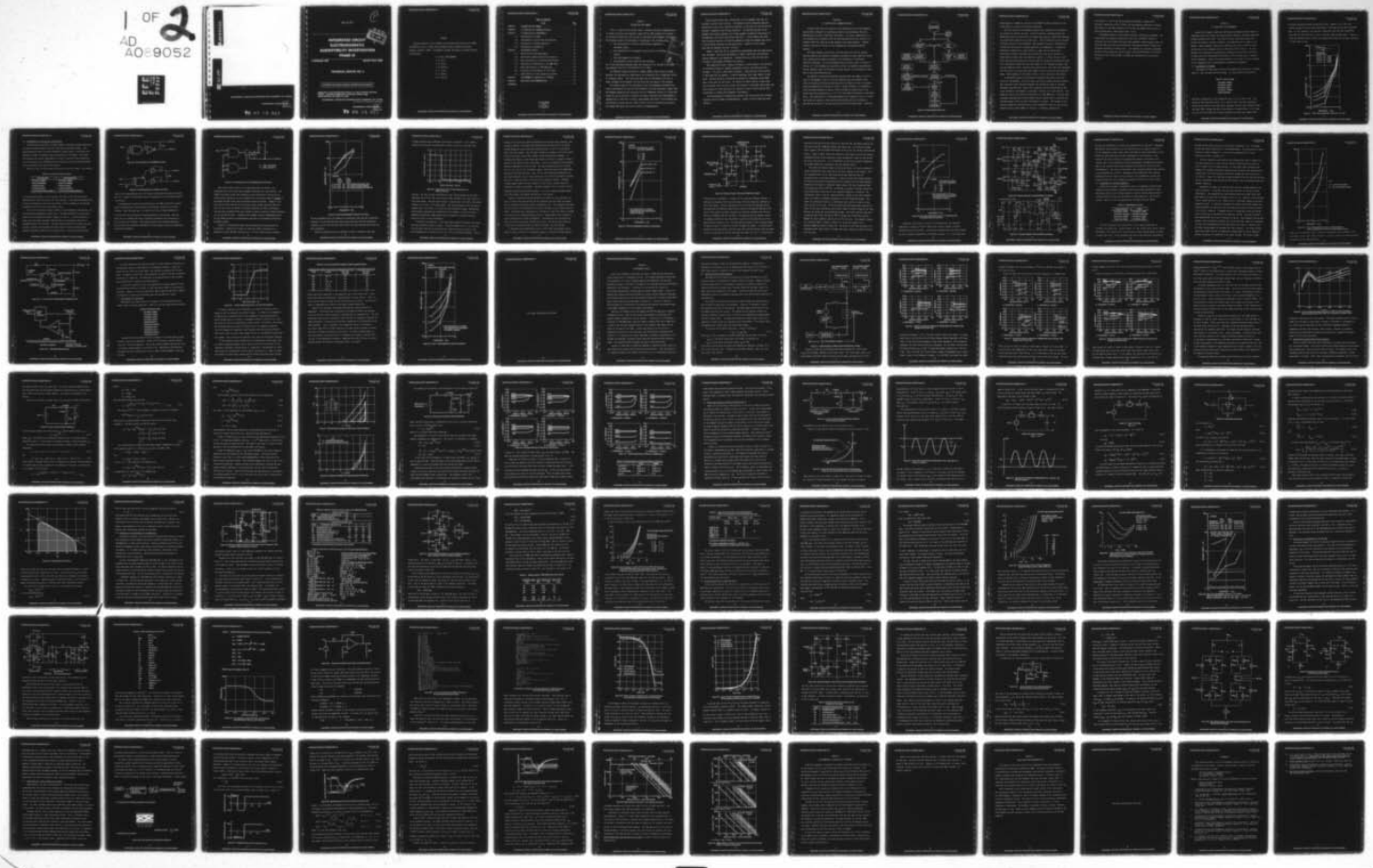

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INTEGRATED CIRCUIT SUSCEPTIBILITY

REPORT MDC E1998

COPY NO. 62

INTEGRATED CIRCUIT ELECTROMAGNETIC SUSCEPTIBILITY INVESTIGATION PHASE III

5 JANUARY 1979 **REPORT MDC E1998**

TECHNICAL REPORT NO. 3

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SUBMITTED TO THE CONTRACTING OFFICER, U.S. NAVAL SURFACE WEAPONS CENTER – DAHLGREN LABORATORY, DAHLGREN, VIRGINIA, 22448 UNDER CONTRACT NO. N60921-76-C-A030

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PREFACE

The work reported in this document was performed under Contract No. N60921-76-C-A030 for the U. S. Naval Surface Weapons Center, Dahlgren Laboratory, Dahlgren, Virginia 22448. The McDonnell Douglas Astronautics Company personnel involved were:

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CHAPTER 1

INTRODUCTION AND SUMMARY

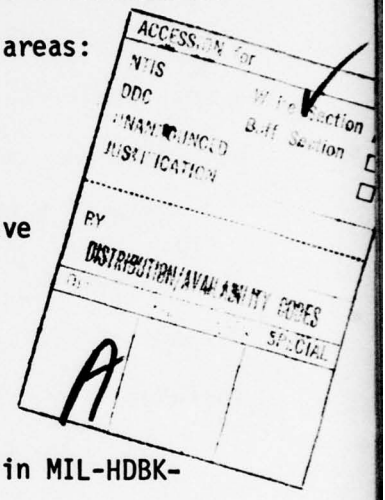
The U. S. Naval Surface Weapons Center - Dahlgren Laboratory (NSWC/Dahlgren) is tasked to provide electromagnetic compatibility (EMC) guidance for designers of electronic systems that must operate in high power electromagnetic environments. The program involves the development of technology in the following areas:

a. the susceptibility of discrete semiconductor components to microwave signals,

b. the susceptibility of integrated circuits (IC's) to microwave signals,

c. the electromagnetic environment,

d. electromagnetic pickup (coupling) and shielding.



All of the technology developed under this program will be included in MIL-HDBK-253 (Appendix) which will be published by U. S. Navy.

The McDonnell Douglas Astronautics Company (MDAC), under contract to NSWC/Dahlgren, has developed the technology on the susceptibility of integrated circuits to microwave signals. This report describes the work performed in the last of three increments which together form the third and last phase of this program.

The primary output of the Integrated Circuit Electromagnetic Susceptibility (ICES) Investigation has been the ICES Handbook[1], which was published 1 August 1978. The handbook summarizes the susceptibilities of integrated circuits in a simplified format for use by electronics designers and others concerned with electromagnetic compatibility of electronic systems. Approximately 500 copies of the handbook were distributed to persons who have shown interest in the IC susceptibility program, and another 200 copies were mailed directly to NSWC/Dahlgren.

Several modifications were incorporated in the IC Handbook that were not included in earlier draft versions. The handbook contains additional measured susceptibility data, with significant expansions in the data for line drivers and receivers, comparators and voltage regulators. The modeling sections of the handbook were greatly expanded, and include examples of modeling interference in TTL NAND gates and bipolar operational amplifiers. A brief chapter was added which discussed coupling and shielding phenomena to make the handbook more nearly a self-contained reference for EMC applications. Chapter 2 of this report describes the handbook revisions in detail.

Chapter 3 describes the IC susceptibility measurements that were made during this increment. Testing was performed on op amps, line drivers and receivers, voltage regulators, and comparators. Susceptibility data from the tests were included in the handbook susceptibility section.

Much modeling activity, ranging from models of rectification in PN junctions to interference models of complete integrated circuits, occurred during this increment. This work is described in Chapter 4. Rectification in PN junctions is described with two methods: a Fourier technique, and a much simpler circuit model. Detailed accounts of modeling interference in integrated circuit NAND gates and op amps are also given. An analysis of signal quality in data transmission systems involving line drivers and receivers is described, which shows that data transmission rates may have to be reduced in order to ensure quality data transmission in intense electromagnetic environments.

Two electromagnetic susceptibility seminars were held during this increment, sponsored jointly by MDAC and NSWC/Dahlgren. Chapter 5 briefly describes these seminars.

CHAPTER 2

IC SUSCEPTIBILITY HANDBOOK REVISION

In August 1978, the final version of the Integrated Circuit Electromagnetic Susceptibility Handbook[1] was completed and mailed to approximately 500 users. NSWC/Dahlgren received an additional 200 copies. This report summarized all of the susceptibility information which had been obtained during this contract in a handbook format for ready use by EMC engineers and system designers. Comments received from earlier versions of this handbook were incorporated wherever possible.

The latest Handbook version used a revised format over earlier versions. Separate chapters were devoted to component susceptibility data, modeling information, coupling and shielding information, and information on interference reduction techniques. The system hardening task flow chart, shown in Figure 2.1 (Figure 2.2 in the Handbook) was modified to reflect the Handbook reorganization. The new flowchart shows clearly where different sections of the handbook are best used in the system hardening task.

The chapter on coupling and shielding considerations was added as an aid to users of the Handbook, since in a typical hardening task the expected pickup levels and expected shielding must be measured or estimated in order to evaluate system susceptibility to external RF fields. Enough information is presented to allow the system designer to make an initial estimate of pickup levels in his system using the relationship $A_e = 0.13\ \lambda^2$ for the effective aperture of unshielded wires. This relationship is a good approximation for frequencies from 1 to 10 GHz. The statistical aspects of both coupling and shielding are also stressed to describe the variations of pickup with wire position and aspect angle. Shielding

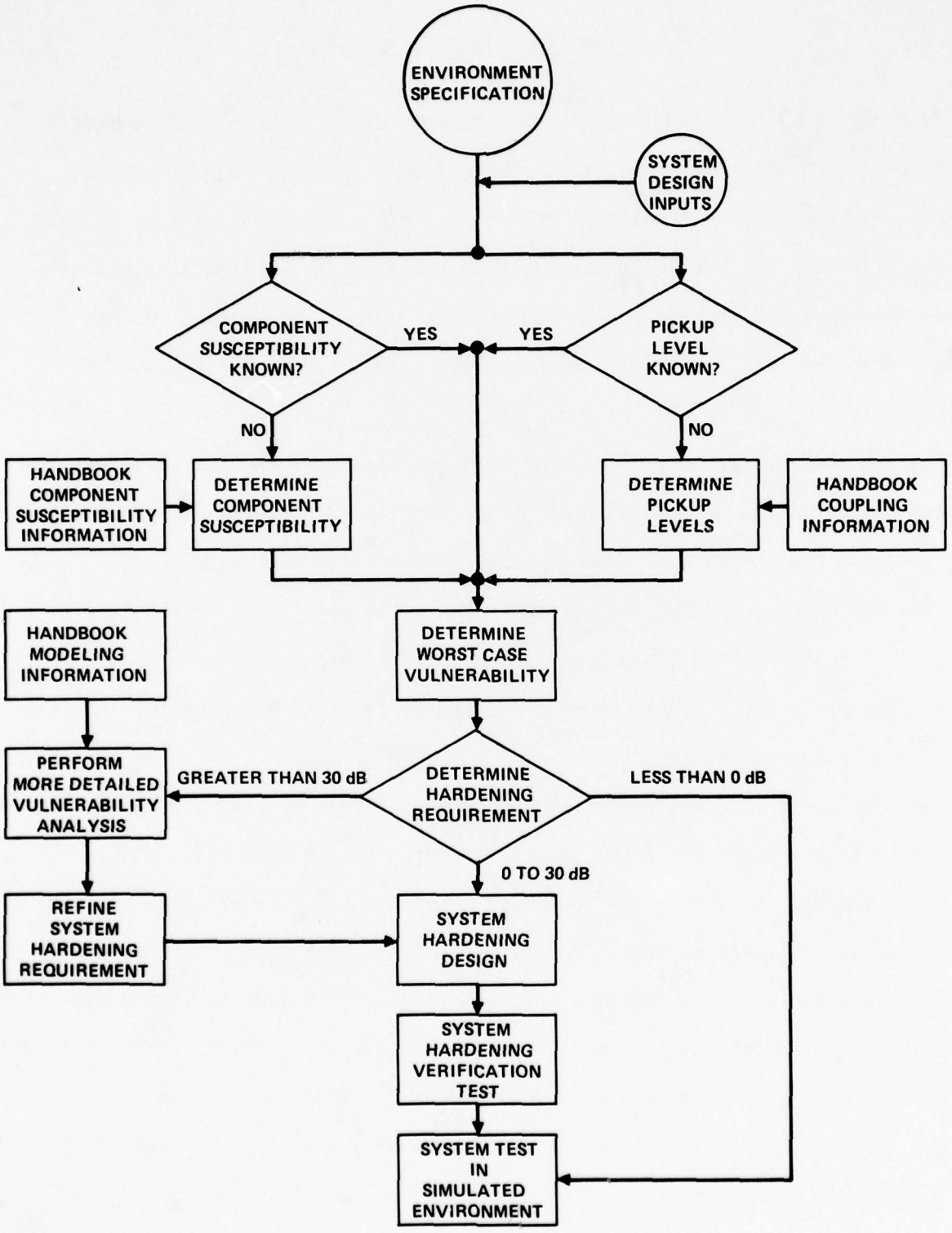


Figure 2.1. System Hardening Task Flow

effectiveness is treated as a shift in the probability density function of the pickup level of a wire with and without shielding.

The final version of the handbook contains much susceptibility information not contained in earlier versions. A short discussion of package effects was added which explicitly states that no package type shows any significant advantage in susceptibility reduction over other types. (This information was not included in earlier versions of the Handbook). New susceptibility data is presented for line drivers and receivers, voltage regulators, and comparators. In addition, theoretical information on signal quality vs. data rate for digital data transmission systems illustrates that reduced data rates may be necessary to ensure quality signals when interference is present. A slight revision in the worst case op amp susceptibility curve was made to include new susceptibility data at 9.1 GHz (which lowered the worst case levels at this frequency by about 4 dB). From the modeling efforts, theoretically predicted worst case levels were developed for TTL devices, and these levels were added to the TTL worst case susceptibility graph. These changes are described in detail in later sections of this report.

A considerable amount of new modeling information was added to the final version of the Handbook. While the diode rectification model and modified Ebers-Moll transistor model remained unchanged, the theoretical ranges of the model parameters were modified. (Worst case information which was developed too late to be included in the Handbook is contained in Section 4.3 of this report). Also added was a worst case study of interference in a 7400 NAND gate. The study used previously developed rectification models and the program SPICE to calculate the minimum RF power levels at which interference is possible. The program is also used to compare the susceptibilities of the standard TTL family to the low power (74L00) and high speed (74H00) TTL families. A modeling simulation of

interference in a 741 op amp was performed using ISPICE, a commercially available timesharing version of SPICE, and macromodeling techniques to analyze interference at the input terminals of an op amp, and compare these results to those obtained when a simple offset model is used.

The Handbook chapter on interference reduction techniques was expanded. The effectiveness of component screening to choose less susceptible devices is discussed, with the ultimate conclusion that component screening can be used, but should be used only after more conventional interference reduction schemes are attempted (shielding, filtering, etc.). The Handbook also contains an expanded section on less susceptible circuit designs, which describes many of the options available to the circuit designer to reduce the susceptibility of electronic circuits.

CHAPTER 3

IC SUSCEPTIBILITY MEASUREMENTS

During this increment, additional testing was performed on several types of integrated circuits to verify, and refine wherever possible, previously published minimum susceptibility levels. The results of tests involving op amps, line drivers and receivers, voltage regulators, and comparators are included in this chapter. Where necessary, special test techniques were used in order to assess the ability of the integrated circuit to function with RF stimulus. For some devices, only a modicum of susceptibility information was previously available, so these tests have contributed significantly to the available body of susceptibility information. Much of the data presented in this chapter is also contained in the Integrated Circuit Electromagnetic Susceptibility Handbook[1].

3.1 Interference in Op Amps

Five types of op amps were tested for RF susceptibility during this increment. Table 3.1 lists the types that were tested. All were tested in an inverting

Table 3.1. Op Amps Tested

NATIONAL LM108A
NATIONAL LM201A
NATIONAL LM207
NATIONAL LH0042C
SIGNETICS NE531

amplifier configuration at the frequencies 0.22, 3.0, 5.6, and 9.1 GHz. Five devices of each type were tested. As in previous tests, the most susceptible condition was found to occur when RF was conducted into the input terminals, where the input offset voltage was used as the measure of susceptibility. In all cases at 0.22, 3.0 and 5.6 GHz, the minimum susceptibility levels were greater than

previously published minimum susceptibility data. However, at 9.1 GHz, the minimum susceptibility level was approximately 4 dB below the previously published data. At this frequency, the type 207 op amps were found the most susceptible, with only 42.6 mW sufficient to cause a 0.05 volt input voltage offset. Figure 3.1 shows the complete graph of worst case susceptibility values for op amps, including all data taken to date.

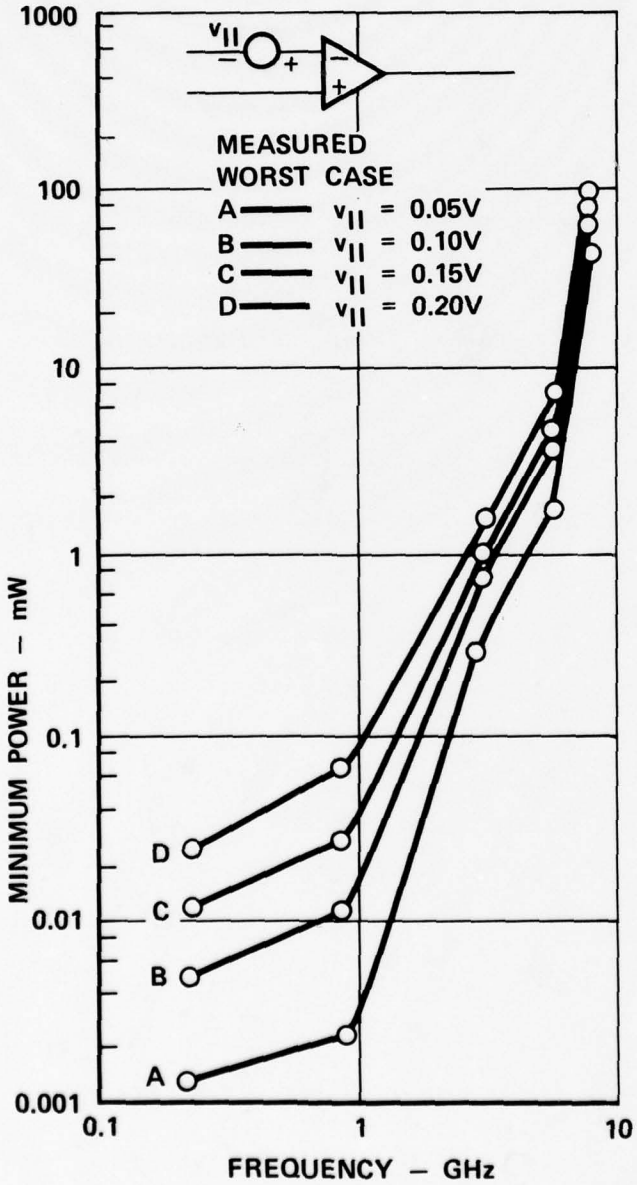


Figure 3.1. Worst Case Susceptibility Values for Op Amps

3.2 Interference in Line Drivers and Receivers

Line drivers and receivers are fairly common in aerospace systems, where they are used to transmit digital data over long system interconnect cables. This section describes tests that were performed on several types of line drivers and receivers in order to determine their susceptibility to RF energy. The drivers and receivers were tested independently in order to single out those characteristics of each which, when altered by RF, would adversely affect system performance (such as decreasing the system noise margin).

Table 3.2 lists the line drivers and receivers that were tested. Five devices

Table 3.2 Line Drivers and Receivers Tested

LINE DRIVERS	LINE RECEIVERS
NATIONAL DS8830	NATIONAL DS8820
SIGNETICS DM8830	SIGNETICS DM8820
FAIRCHILD 9614	FAIRCHILD 9615
FAIRCHILD 55109	FAIRCHILD 55107A
TEXAS INSTRUMENTS SN55110	TEXAS INSTRUMENTS SN55107A

of each type were tested. In this section, the tests of the line drivers are described first, then the tests of the line receivers. The minimum susceptibilities of each are combined at the end of the section to yield estimates of the minimum susceptibility of line driver and receiver pairs.

All of the line drivers listed in Table 3.2 are differential line drivers, i.e., each drives two complementary output lines. The 8830 and 9614 line drivers were tested in the configuration shown in Figures 3.2 and 3.3. A resistor placed in shunt across the output terminals simulated the line terminating resistors on the 8820 and 9615 line receivers. The type 55109 and 55110 line drivers have open collector (current type) outputs and require pullup resistors on each output terminal (the 8830 and 9614 contain active pullups). The pullup resistors were

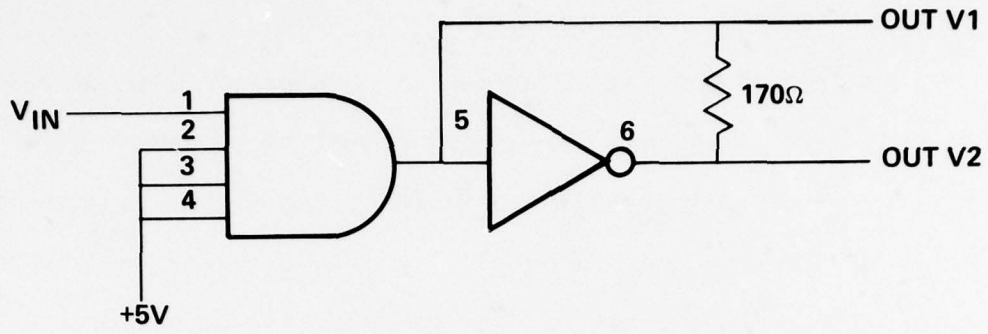


Figure 3.2. Test Configuration for Type 8830 Line Drivers

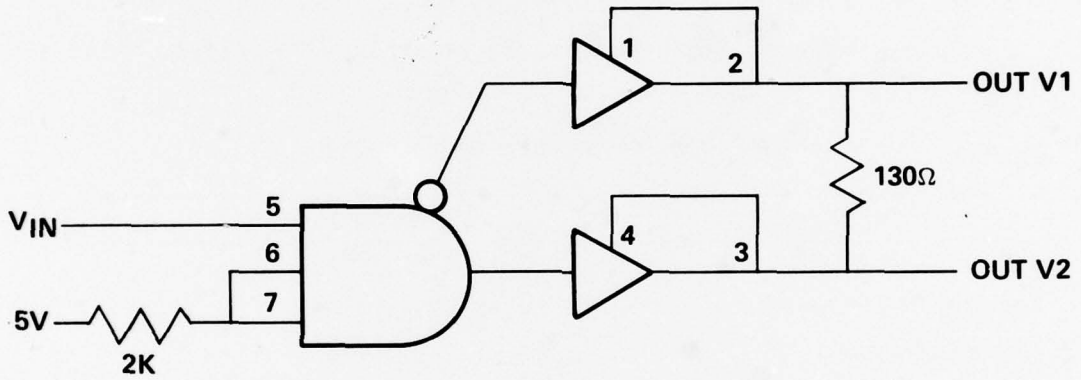


Figure 3.3. Test Configuration for Type 9614 Line Drivers

chosen to give approximately zero volts output voltage when the output transistor was "on". Figure 3.4 illustrates the test configuration for the 55109 and 55110 line drivers.

Susceptibility criteria were established for the 8830 and 9615 line drivers based on manufacturers' specifications for the output voltage at each output terminal. When the output was in a nominal low state, voltage thresholds of 0.4, 0.8, and 2.0 volts defined increasing degrees of interference. When the output was in a nominal high state, increasing interference was defined by 2.4, 2.0, and 0.8 volt thresholds. Each output terminal was considered separately, and the device was considered susceptible if either output crossed the appropriate interference threshold.

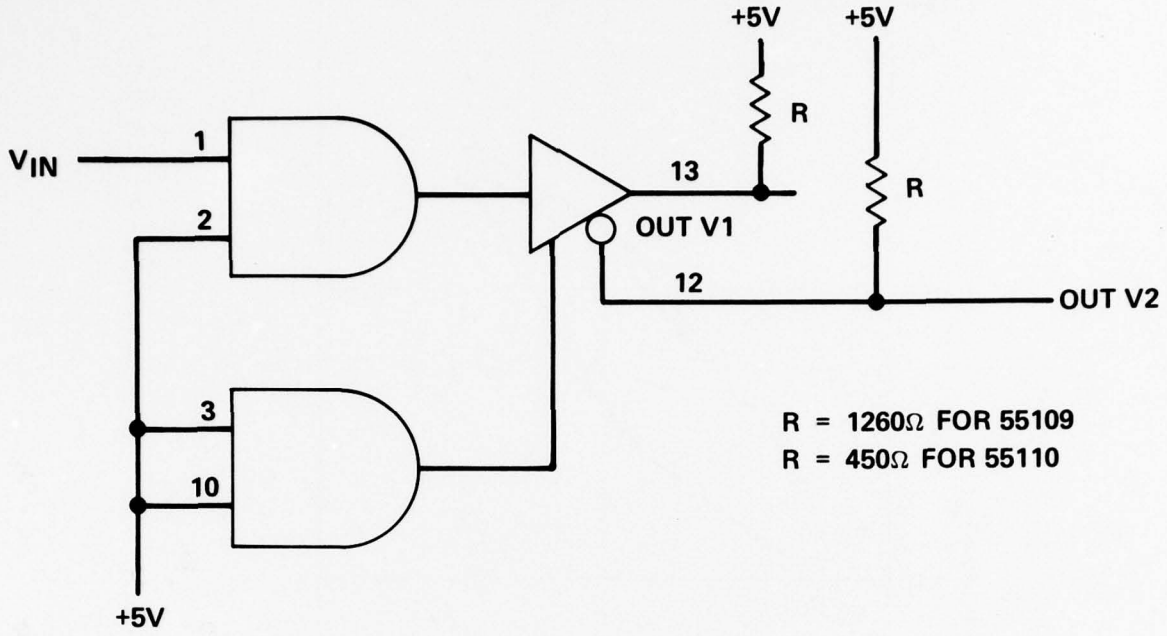


Figure 3.4. Test Configuration for Type 55109 and 55110 Line Drivers

Due to the current outputs of the 55109 and 55110 line drivers, the susceptibility criteria were chosen somewhat differently for these devices. The nominal low output current was discovered to vary from device to device due to normal process variations, so the susceptibility criteria were based on changes in the output voltages rather than on absolute voltage thresholds. Changes of 0.4, 0.8, and 2.0 volts from the no RF low state output voltage (which was near zero volts in the circuit of Figure 3.4) defined increasing low state interference. The high state susceptibilities were defined in terms of absolute voltage thresholds at 2.4, 2.0 and 0.8 volts. Therefore, the voltages at which interference occurs for the 55109 and 55110 are approximately the same as the thresholds defined for the 8830 and 9614.

Figure 3.5 illustrates the worst case susceptibility values measured for line drivers. Inspection of Figure 3.5 shows the drivers susceptible to a minimum of 12 mW at 220 MHz, using the 0.4 - 2.4 volt output voltage threshold.

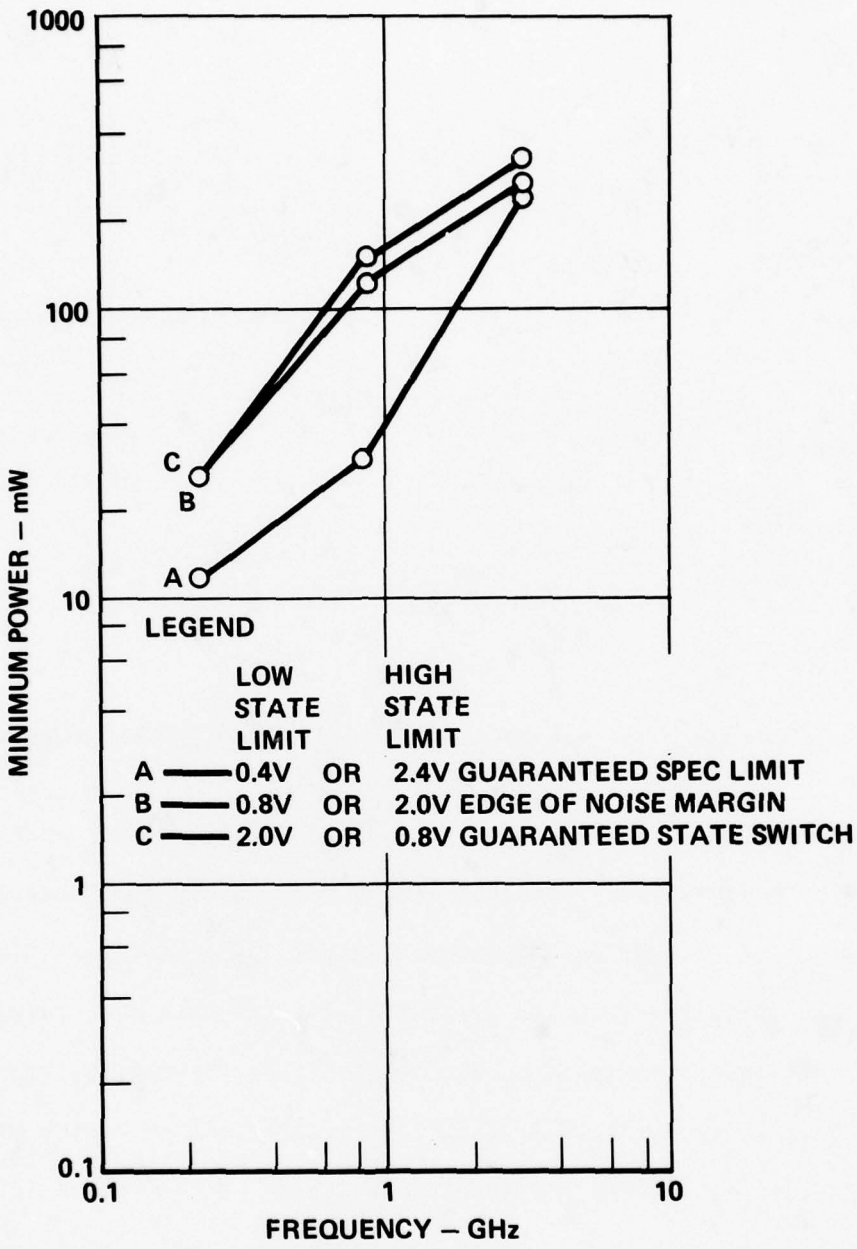


Figure 3.5. Worst Case Susceptibility Values for Line Drivers

For the type 8830 drivers the outputs and ground were found the most susceptible terminals; for the 9614 the power supply and ground were the most susceptible terminals; and for the 55109 and 55110 drivers the input terminals were found the most susceptible.

Receiver susceptibilities were defined in terms of changes in the input

voltage threshold which determines the receiver switchpoint. As an example, Figure 3.6 illustrates the input-output transfer curve for a type 9615 line

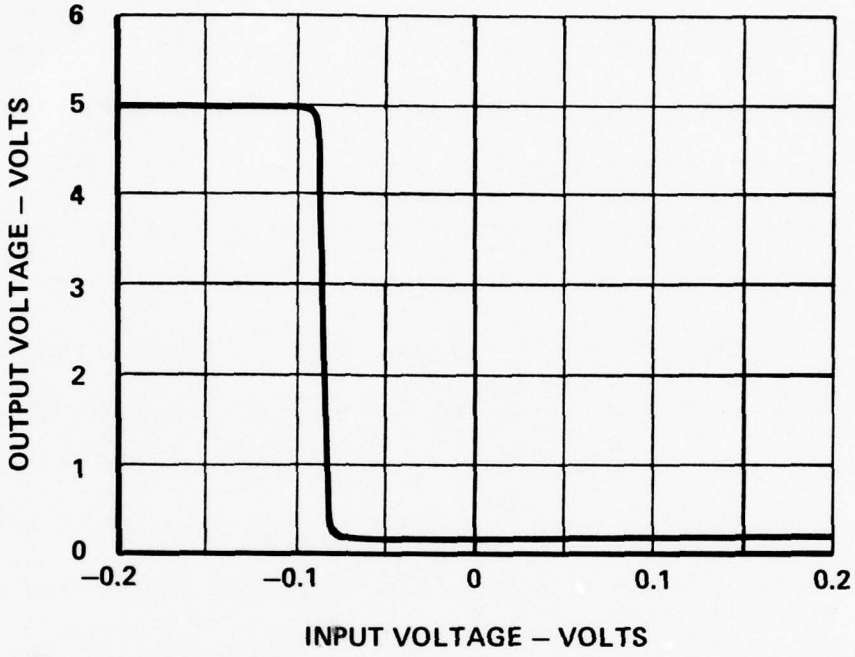


Figure 3.6. Typical Input–Output Transfer Characteristic for 9615 Line Receiver

receiver. At input voltages (differential input voltage between the two input terminals) below -0.08 volts, the receiver output voltage is 5.0 volts, which is a high state output. When the input voltage is greater than -0.08 volts, the output voltage is 0.2 volts, a low state output. The input voltage at which the output changes state, -0.08 volts, is called the input threshold voltage. Manufacturer specifications guarantee this threshold will lie between -0.5 and +0.5 volts. A threshold outside this range reduces the noise margin of the device and may cause bit errors in noisy environments.

In testing line receivers, it was found that conducted RF energy could cause the input threshold voltage to change. Threshold changes of 0.5, 1.0, 2.0, and 5.0 volts were used for the susceptibility criteria during the testing. The test procedure was as follows (to test for a 0.5 volt threshold change): first a

voltage of +0.5 volts was applied differentially across the input terminals, and increasing amounts of RF power were conducted into the device until an output voltage change was noted (indicating susceptibility), or until the maximum RF power limit was reached. Then the input voltage was changed to -0.5 volts (which switches the output to the other state), and the procedure was repeated. If increasing RF induces a state change when either a positive or negative voltage is applied at the input terminals, the effect is that of an apparent input threshold change of magnitude 0.5 volts or more. The same procedure was used in testing for 1.0, 2.0, and 5.0 volt threshold changes. During the tests, the common-mode voltage at the inputs was zero. Thus, for 0.5 volts applied differentially at the input terminals, the (+) input was held at +0.25 volts with respect to ground, and the (-) input was held at -0.25 volts with respect to ground. Threshold voltage changes reduce the noise immunity of the circuit, and may cause poor operation in certain environments. Threshold changes of 0.5, 1.0, and 2.0 volts represent decreasing system noise margins. A 5.0 volt threshold change denotes zero noise margin, and probable malfunction of the device.

Figure 3.7 shows the minimum susceptibility levels for line receivers, all points of which were measured when RF was conducted into the strobe or response control terminals which were the most susceptible ports. The susceptibility levels for the 2.0 and 5.0 volt thresholds are nearly the same, so only three curves are shown. The devices were susceptible to a minimum of 1.0 mW of RF power at 220 MHz using the 0.5 volt threshold change criterion. Greater powers were required to cause susceptibility at higher frequencies. Interestingly, the susceptibility levels are nearly the same at 910 MHz and 3.0 GHz. The devices were tested at 5.6 GHz, but no susceptibility was noted at RF powers less than 400 mW.

To determine why susceptibility occurs at the strobe and response control, refer to Figure 3.8 which is a schematic diagram of a National DS 8820 receiver.

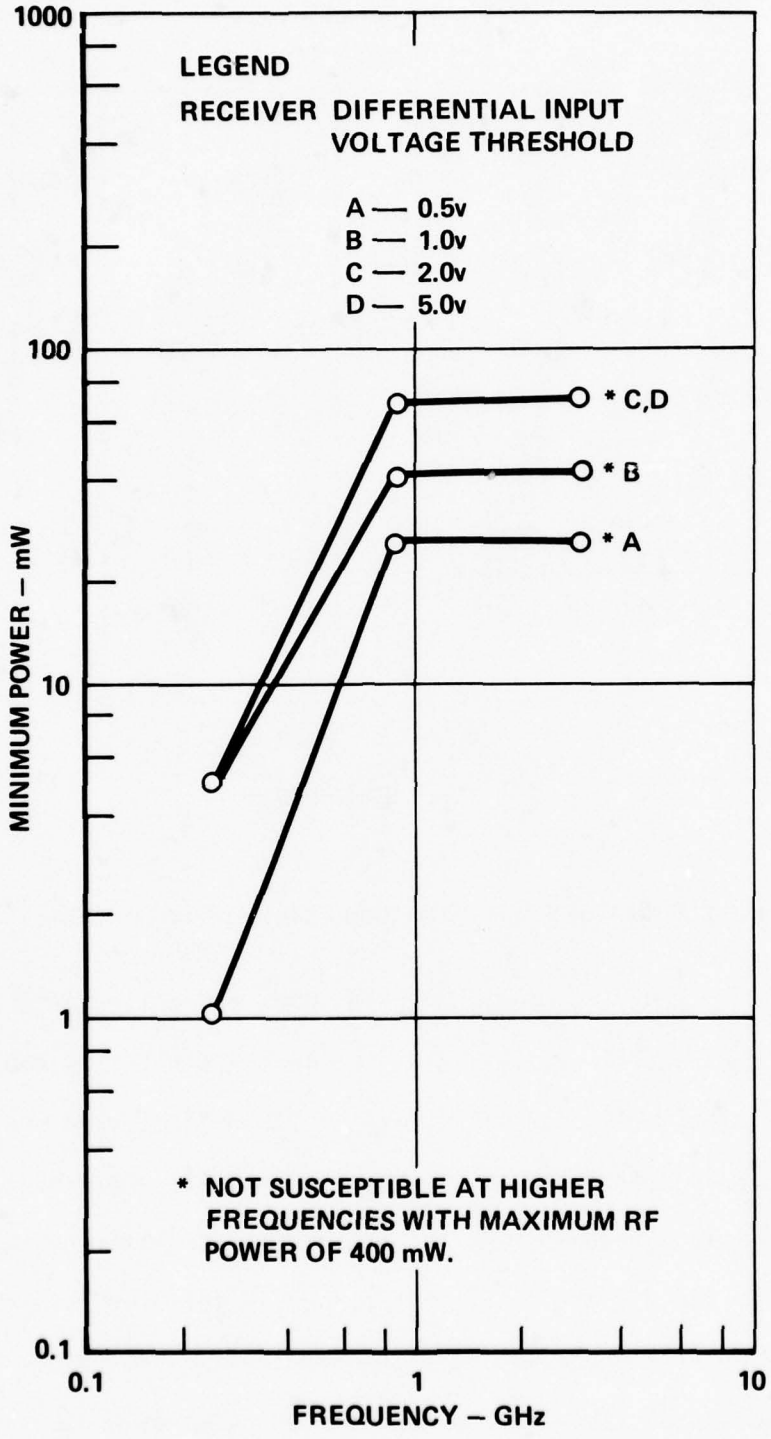


Figure 3.7. Worst Case Susceptibility Values for Line Receivers

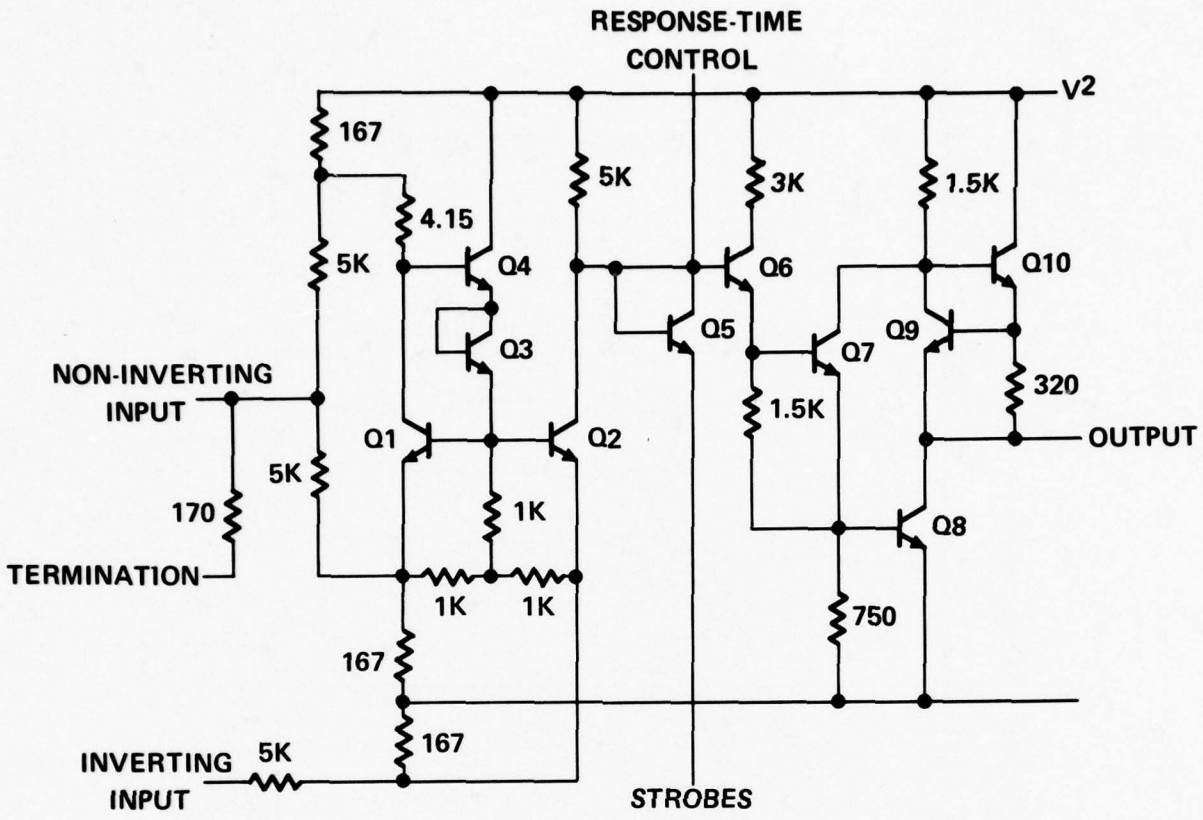


Figure 3.8. Schematic Diagram of National DM 8820 Line Receiver

Transistor Q5 is connected as a diode, with its base and collector shorted. In testing, the response control was left open, while the strobe was connected to the 5 volt supply. The most susceptible case at 220 MHz occurred when RF was conducted into the response control while a positive voltage was applied at the input, which causes the output voltage to be high (the transfer curve for this device is different than for the 9615). RF conducted into the response control is probably rectified at the base-emitter junction of transistor Q6, or at the base-collector junction of Q2. The base-emitter junction of Q5 is reverse biased by about 4.5 volts, so would not rectify low power RF signals. If rectification occurred at the base-emitter junction of Q6, the rectified current could be enough to turn on transistor Q7 and Q8, switching the output to a low. If rectification

occurred at the base-collector junction of transistor Q2, the effect would be the same as RF entering a NAND gate output with output low: the collector voltage would increase, and may become high enough to turn on Q6, Q7, and Q8, switching the output. Higher RF power levels were required at the strobe to switch the output, presumably because the RF energy has to pass through Q5 in order to reach Q2 and Q6, with a resulting loss. It is interesting to note that at higher frequencies the strobe becomes more susceptible than the response control.

The strobe and response controls, unlike the inputs, are rarely connected to system interconnect lines, which may be the major receptors of RF energy. Thus, the susceptibilities of the input ports may be more important than the susceptibilities of the other terminals. Figure 3.9 shows the minimum susceptibilities of the receivers considering only RF conducted into the input terminals. Comparison with Figure 3.7 shows the inputs roughly 5 dB less susceptible than the response and strobe terminals. At 220 MHz, a minimum 2.5 mW was required to cause interference, using the 0.5 volt threshold change as a criterion. The interference effect is due to a rectified offset voltage at the input terminals. Figure 3.10 shows the schematic diagram for a Fairchild 55107A receiver. The inputs are connected directly to a differential pair, which is similar to the input circuit of an op amp. RF can be rectified by the base-emitter junction of either of the input transistors, which would induce an offset voltage at the input terminal and change the input threshold voltage. The 55107A receivers were more susceptible than either the 9615 or 8820's, because the latter have resistors between the input terminals and the rest of the circuitry. The schematic diagram for a Fairchild 9615 is shown in Figure 3.11, while the schematic for a National DS8820 was shown in Figure 3.8. The effect of the input resistors is to attenuate the RF signal before it reaches the input transistors, where rectification can occur.

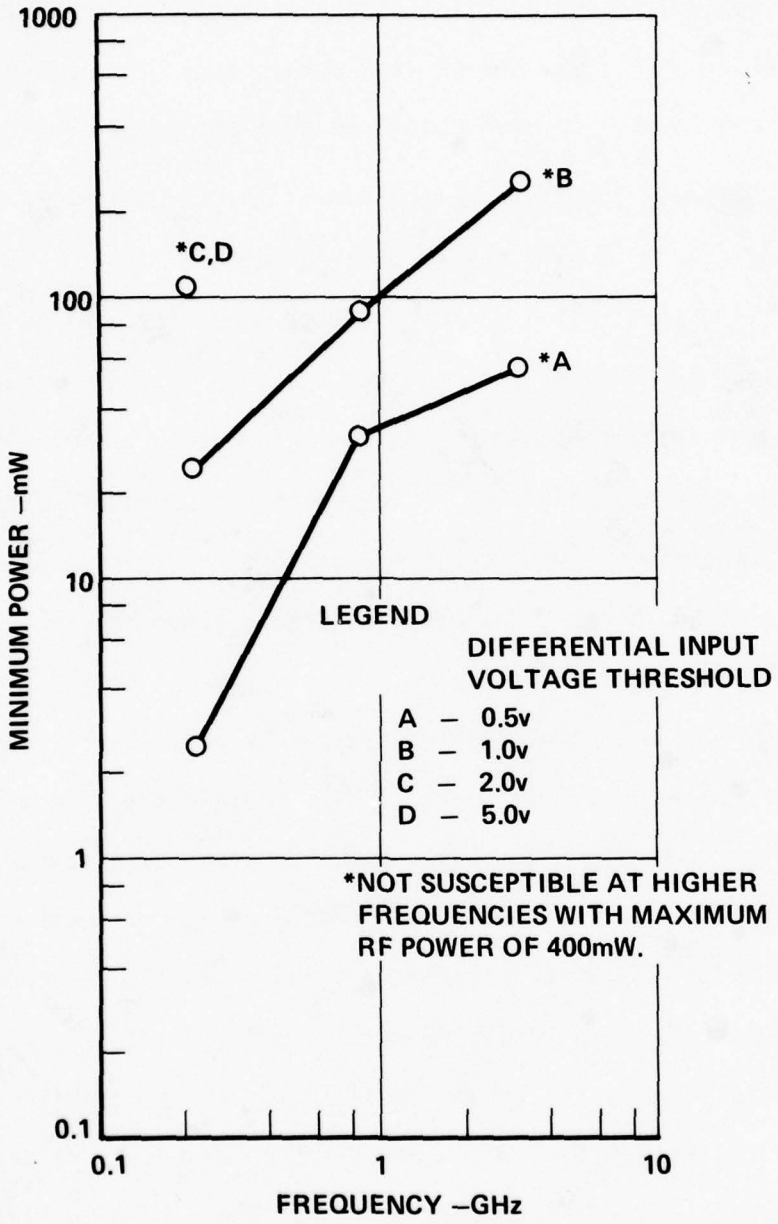


Figure 3.9. Worst Case Susceptibility Values for Line Receivers with RF Entering Input Terminals Only

Generally, line drivers are used in conjunction with line receivers. Comparison of Figures 3.5 and 3.7 shows line receivers roughly 7 dB more susceptible than line drivers. (Line driver susceptibility lies within roughly 0.5 dB of receiver susceptibility at 910 MHz, however). If a line driver and

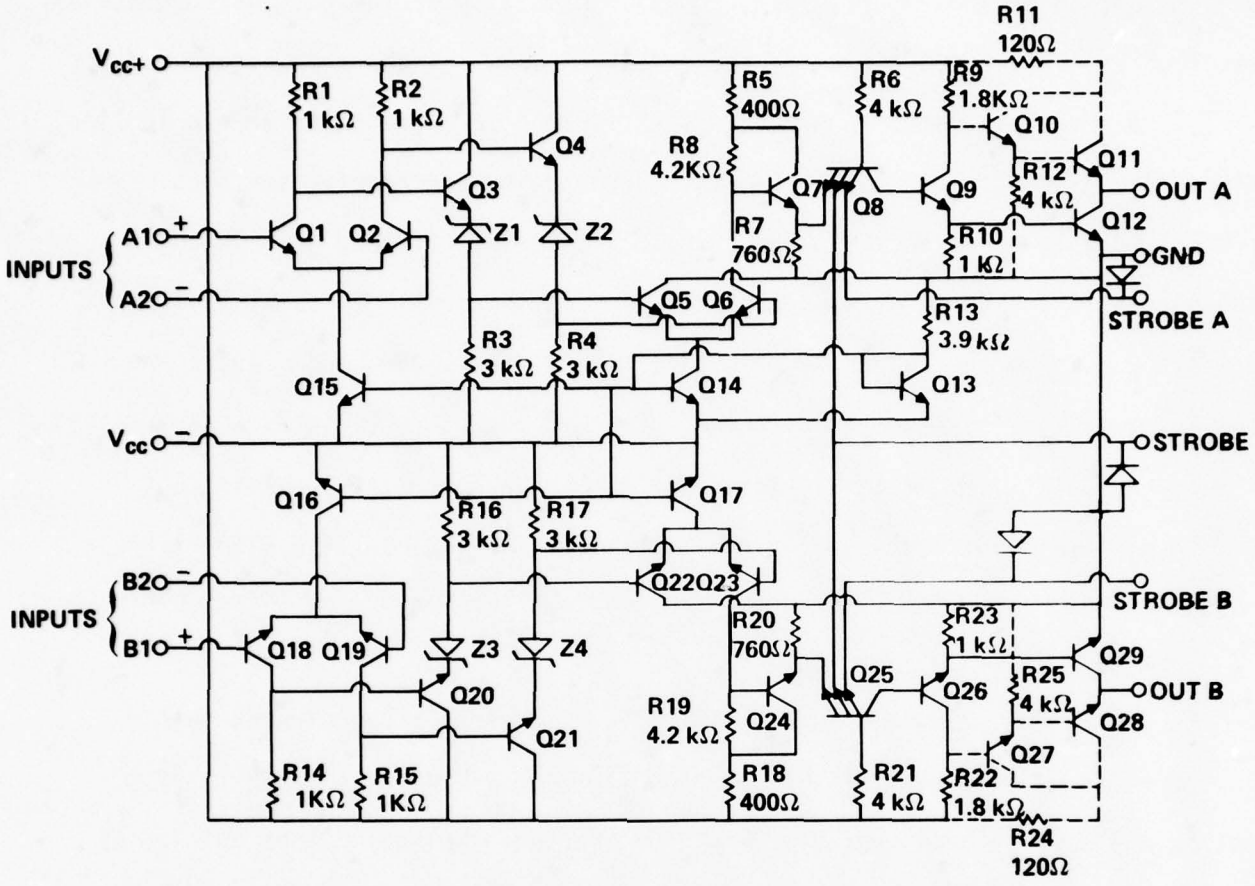


Figure 3.10. Schematic Diagram of Fairchild 55107A Line Receiver

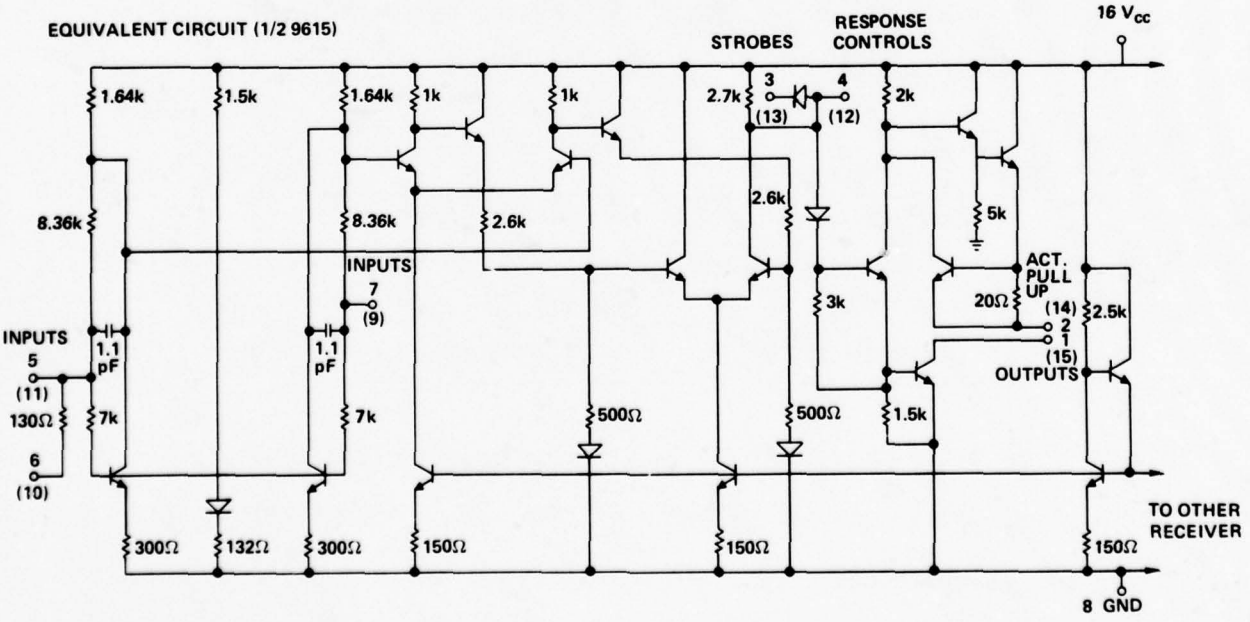


Figure 3.11. Schematic Diagram of Fairchild 9615 Line Receiver

receiver are considered as a system, the susceptibility of the pair is adequately described by the susceptibility of the receivers only, as shown in Figure 3.7. For all frequencies tested, power levels sufficient to cause interference in line drivers are also sufficient to cause interference in line receivers. Thus Figure 3.7 was used to define the susceptibility levels of line drivers and receiver pairs in the Integrated Circuit Electromagnetic Susceptibility Handbook, where it was relabeled "Worst Case Susceptibility Values for Line Drivers and Line Receivers". The receiver differential input voltage thresholds were retained as the susceptibility criteria. Knowledge of the differential input voltage threshold allows the signal quality (jitter) to be estimated for a given line length and data rate from information presented in Section 4.7 of this report.

3.3 Interference in Voltage Regulators

During this increment, susceptibility tests of integrated circuit voltage regulators were performed to supplement earlier published susceptibility data. Testing was done on 3-pin voltage regulators having a nominal output voltage of 5 volts (earlier testing had concentrated on these regulators), and on 8-pin devices. Table 3.3 lists the manufacturers and types that were tested.

Table 3.3. Voltage Regulators Tested

3-PIN (5 VOLTS)	8-PIN
NATIONAL LM309	FAIRCHILD μA305
MOTOROLA MLM309	MOTOROLA MLM305
MOTOROLA 78M05	NATIONAL LM305
FAIRCHILD 78M05	NATIONAL LM300

The 3-pin regulators were tested with a 7 volt input voltage and six different load conditions: output currents of 1 mA, 20 mA, 50 mA, 100 mA, 150 mA, and 200 mA. The susceptibility criterion was an output voltage below 4.75 volts or above 5.25 volts. RF was conducted into each of the three pins individually;

RF entering the output was found to be the most susceptible case. At 220 MHz, devices were found susceptible to 1.3 mW minimum power. The susceptibility levels increase at higher frequencies. A plot of the susceptibilities of 3-pin regulators is shown in Figure 3.12.

The 8-pin regulators were tested in the configuration shown in Figure 3.13. The input voltage was 18 volts, and the output voltage divider was chosen to yield a nominal 12 volts output voltage. As the actual output voltage varied somewhat for different types due to manufacturing variations, the susceptibility criterion was a 0.25 volt change in the output voltage from the no RF case for that device. Figure 3.12 shows the minimum susceptibilities for the 8-pin devices. The most susceptible cases occurred for RF conducted into the reference bypass and feedback terminals.

Examination of Figure 3.12 indicates that the 8-pin voltage regulators are quite susceptible. At 220 MHz, only 0.07 mW of RF power is required to cause interference. The susceptibility values approach those of op amps, which have been shown to be sensitive to RF powers as low as 1 μW. Analysis of the regulator circuit reveals why this is so. Figure 3.14 is a functional diagram of the basic regulator circuit. In multi-pin regulators the op amp, series pass element, and voltage reference are internal to the chip, while the voltage divider consisting of R_1 and R_2 is external. A feedback circuit is formed that drives the voltage across resistor R_2 to the value of the reference voltage. The output voltage is then determined by the values of resistors R_1 and R_2. The presence of the op amp, however, causes the device susceptibility to be quite high. When RF is conducted into the pins corresponding to the op amp inputs, the signal is rectified, and an offset voltage appears at the amplifier input terminals. The offset voltage upsets the op amp's ability to compare the voltage across R_2 to the reference voltage, resulting in a deviation in the output voltage. The offset voltage

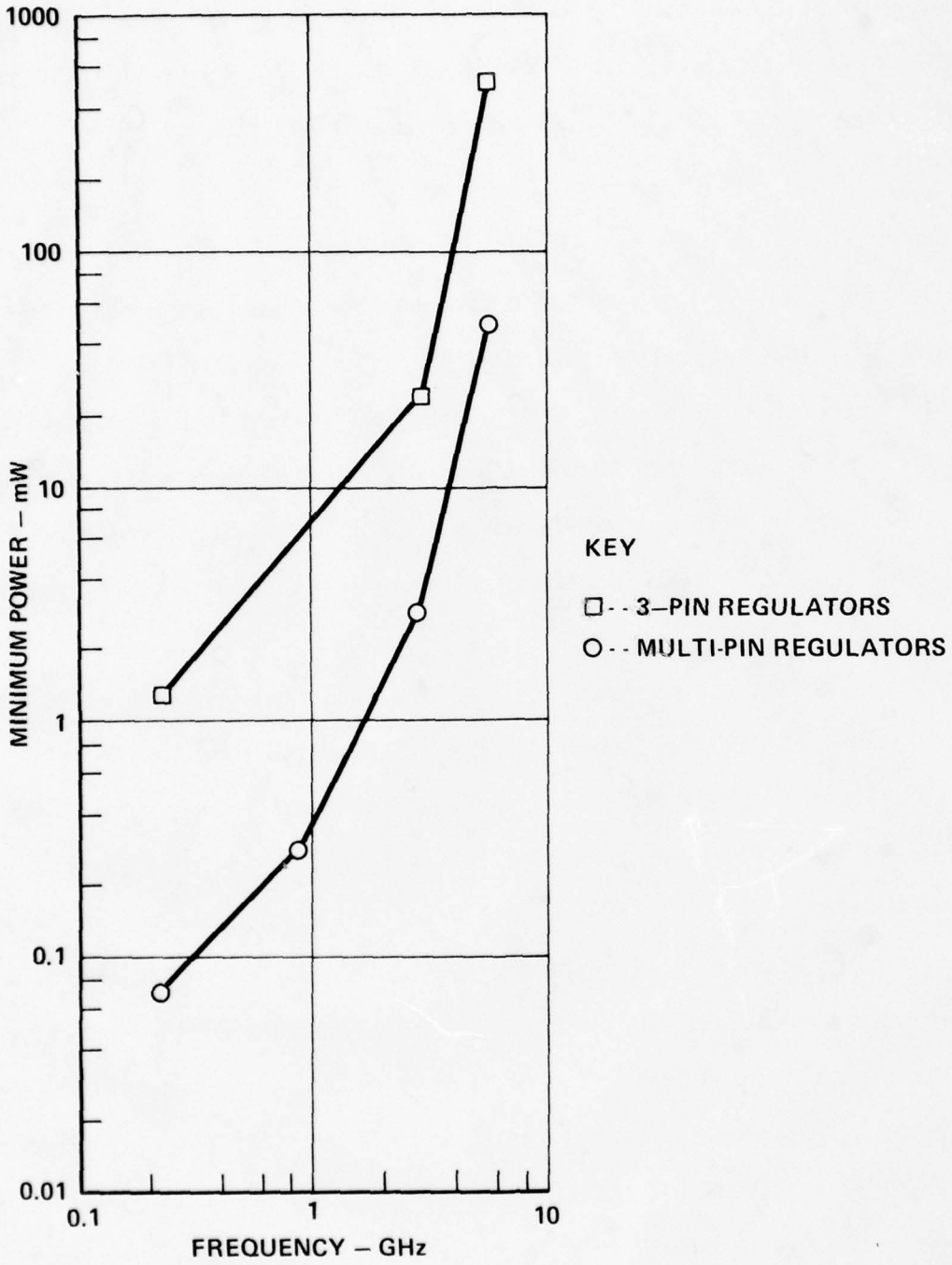


Figure 3.12. Worst Case Susceptibility Values for Voltage Regulators. Output Voltage Change of 0.25 Volt is Susceptibility Criterion.

observed at the amplifier input in multi-pin regulators could be modeled in the same manner as the input offset voltage for op amps by placing an offset generator in series with the input terminals.

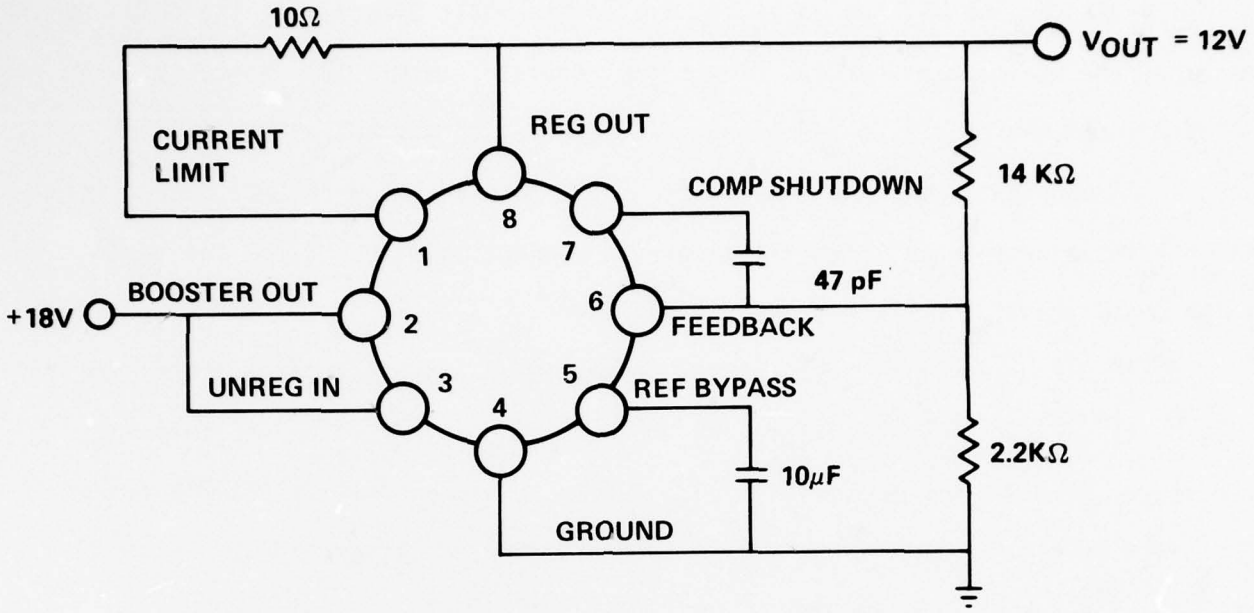


Figure 3.13. Circuit for 8 Pin Voltage Regulator Susceptibility Tests

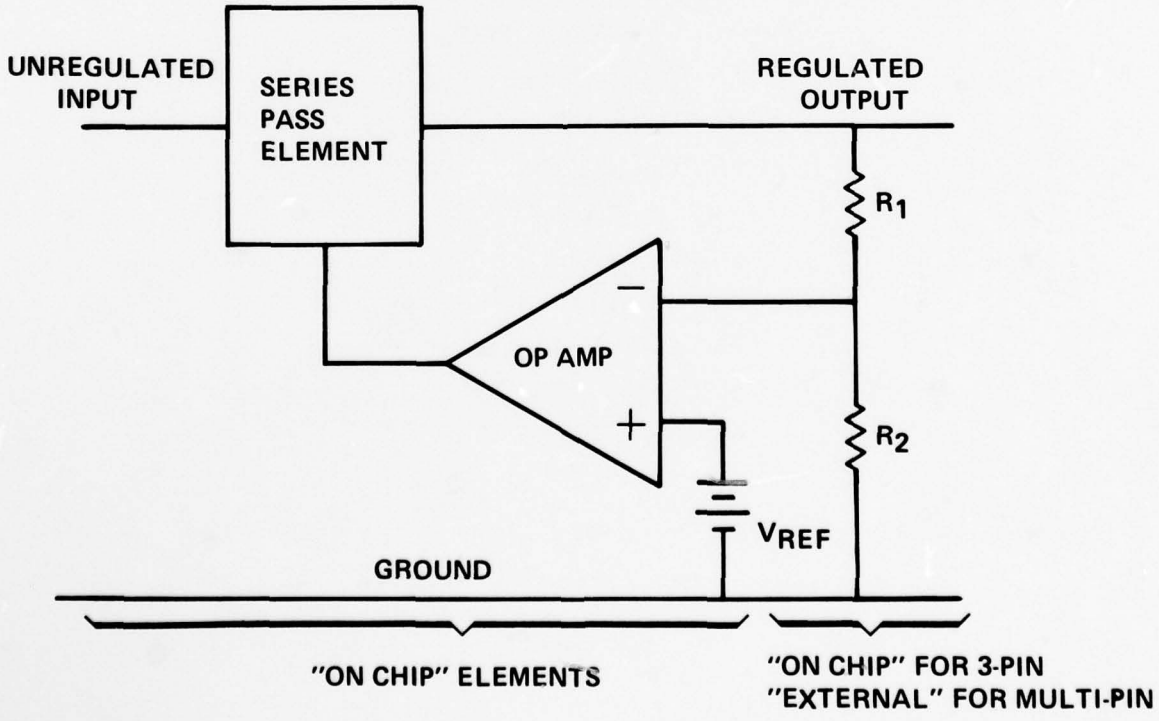


Figure 3.14. Basic Series Regulator Circuit

In 3-pin regulators, the resistive divider is built directly on the chip, so the amplifier inputs are inaccessible at the regulator terminals. Hence, RF cannot directly enter the op amp inputs, and the device susceptibility is much lower. As shown in Figure 3.12, 3-pin regulators are about 12 dB less susceptible than multi-pin regulators. The difference in susceptibilities of the two types may be significant to designers and EMC engineers.

In the 8-pin regulator testing, the compensation and bypass capacitors were located outside the RF test fixture, so that they had no effect on the incoming RF energy. However, in an actual application these capacitors may offer a degree of protection by shunting the RF energy away from the amplifier inputs.

3.4 Interference in Comparators

Measurements were made during this increment of the RF susceptibility of several types of voltage comparators. Table 3.4 lists the types that were tested.

Table 3.4. Comparators Tested

NATIONAL LM306
NATIONAL LM360
FAIRCHILD μA760
NATIONAL LM311
SIGNETICS LM311
MOTOROLA MLM311
FAIRCHILD μA311
SIGNETICS μA710
MOTOROLA MC1710
FAIRCHILD μA710

Susceptibility was defined in terms of changes in the input-output voltage transfer curve of the comparator. Figure 3.15 illustrates a typical transfer curve for a 710 type comparator. The output switches between high and low values at an input voltage between -1.0 mV and +1.0 mV. Manufacturer specifications guarantee that this switching will occur at input voltages between -3.0 mV and +3.0 mV.

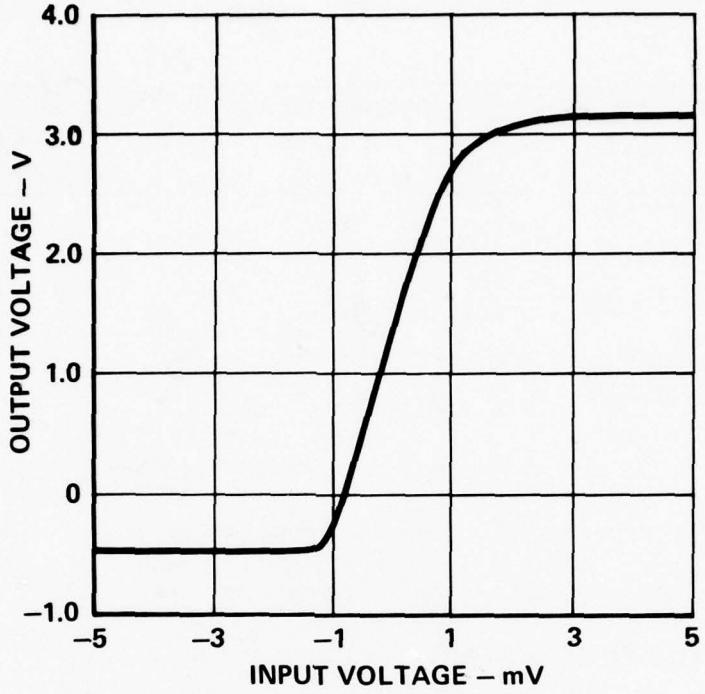


Figure 3.15. Typical Voltage Transfer Curve for Type 710 Comparator

RF energy conducted into the comparator can cause the transfer curve to change so that the comparator switchpoint changes. An offset in the comparator switchpoint has an adverse effect on the comparator's accuracy when used to detect voltage levels in circuits. Switchpoint offsets of +0.05, +0.10, +0.20, and +0.50 volt were the susceptibility criteria used in the testing. The testing was performed (using the +0.05 volt offset case as an example) by applying +0.05 volt between the comparator input terminals and increasing the RF power level until either an output state change occurred, or the maximum RF power level was reached. Then -0.05 volt was applied at the input and the process repeated.

If the comparator output voltage fails to indicate the correct state, then an offset of magnitude greater than or equal to 0.05 volt has occurred in the comparator switchpoint, and the device is susceptible. The procedure is similar when testing for switchpoints of $\pm$0.10, $\pm$0.20, and $\pm$0.50 volt. Table 3.5 shows the maximum low state output voltage and the minimum high state output voltage

Table 3.5. Limits on Output State Voltages for Determining State Changes

COMPARATOR TYPE	SUPPLY VOLTAGES (VOLTS)	MAXIMUM LOW STATE VOLTAGE (VOLTS)	MAXIMUM HIGH STATE VOLTAGE (VOLTS)
306	+12, –6	0.4	2.5
311	+5	0.4	4.0
311	+15, –15	1.0	14.0
360	+5, –5	0.4	2.5
710	+12, –6	0.0	2.5
760	+5, –5	0.4	2.5

which were used to determine if the comparator was in the correct state. These limits were based on manufacturers' specifications for these devices. Table 3.5 also lists the supply voltages at which these devices were tested. Note that the type 311 comparators were tested at two supply voltage combinations.

Figure 3.16 illustrates the minimum susceptibility values observed for comparators. The devices were susceptible to a minimum of 0.025 mW at 220 MHz, using the 0.05 volt offset criterion as the definition of susceptibility. Type 360 comparators were the most susceptible, while the type 311 comparators appeared the least susceptible. The devices were the most susceptible to RF conducted into the input terminals. This is expected, since comparators contain a differential pair input stage similar to that contained in op amps, which are known to be very sensitive to RF power conducted into the inputs. An offset voltage appears at the input terminal into which the RF is conducted, which causes a similar effect to occur in the comparator switchpoint. Modeling this effect utilizes previously proposed methods for modeling interference effects in op amps[1].

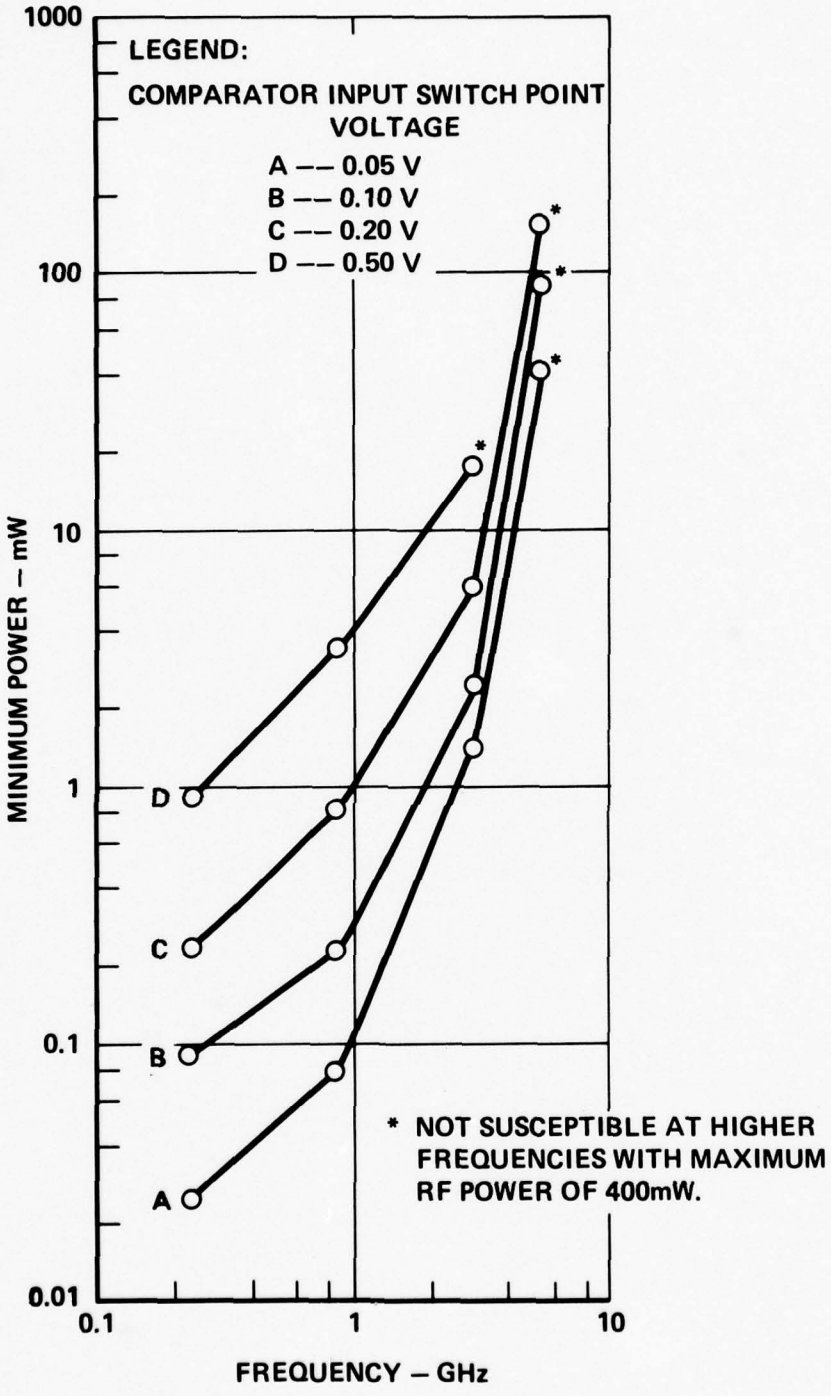


Figure 3.16. Worst Case Susceptibility Values for Comparators

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CHAPTER 4

INTERFERENCE EFFECTS

During this increment, much effort was spent in modeling the interference effects which occur in integrated circuits. This chapter describes the work that was performed in this area, including detailed investigations into the basic mechanisms involved. Sections 4.1 through 4.3 are concerned with the rectification properties of PN junctions. In Section 4.1, the results of a series of rectification measurements are described for several common diodes. Section 4.2 expands the existing rectification theory by using a Fourier expansion technique, and includes predictions of the rectification efficiencies of several diodes which agree closely with the data presented in Section 4.1. Section 4.3 takes an existing model for rectification in PN junctions and predicts the expected range of the model parameters for use in worst case analyses.

Sections 4.4 through 4.6 of this chapter describe the modeling of complete integrated circuits. Most of the circuits were modeled in conjunction with special computer programs for circuit analysis. In Section 4.4, interference is simulated in 7400 NAND gates using the computer program SPICE, and a comparison is made of the relative susceptibilities of the standard, high speed, and low power TTL versions of this gate. A worst case analysis of this circuit is presented in Section 4.5, using the worst case rectification information from Section 4.3. In Section 4.6, several approaches to modeling interference in 741 op amps are presented, including a very simple and convenient offset generator model. The programs ISPICE and SPICE2 are used in the calculations.

Section 4.7 describes an analytical approach to evaluating signal quality in data transmission systems using line drivers and receivers. The signal quality is inversely related to the "jitter" which may occur in a transmitted signal and

this section presents a means of evaluating this quantity. Susceptibility information from Section 3.2 can be combined with the results of this section to yield signal quality information in terms of RF frequency and power level.

4.1 Diode Rectification Measurements

Rectification of RF signals by PN junctions has been determined to be the principal source of interference in modern electronic circuits. However, because of the nonlinear nature of semiconductor junctions, an analytical approach to studying rectification becomes quite involved, except for the small signal case where simplifying assumptions can be made. A study of diode rectification was undertaken during this increment to measure some of the rectification properties of semiconductors.

The current rectification efficiency of several diodes was measured versus bias voltage, RF power level, and frequency. Figure 4.1 illustrates a typical test setup that was used in the testing. The diode under test was placed in an HP 11602B transistor test fixture. The cathode of the diode was placed at RF ground by locating a coaxial short in the RF line an appropriate distance beyond the test fixture socket. The diode was biased with a power supply, and the dc component of diode current was measured with an electrometer. The RF power level was measured with a power meter and directional coupler.

The current rectification efficiency, η (eta), is defined as

$$\eta = (i_{RF} - i_{no\ RF})/P_{RF}, \tag{4.1}$$

where i_{RF} is the dc component of diode current when the RF signal is present,

$i_{no\ RF}$ is the diode current when no RF signal is applied, and

P_{RF} is the RF power level which causes i_{RF} to flow.

The current recitfication efficiency was measured for diode bias voltages of 0, 0.25, 0.50, and 0.60 volts. Frequencies of 220 MHz, 450 MHz, 1 GHz, and 2 GHz were used in the testing.

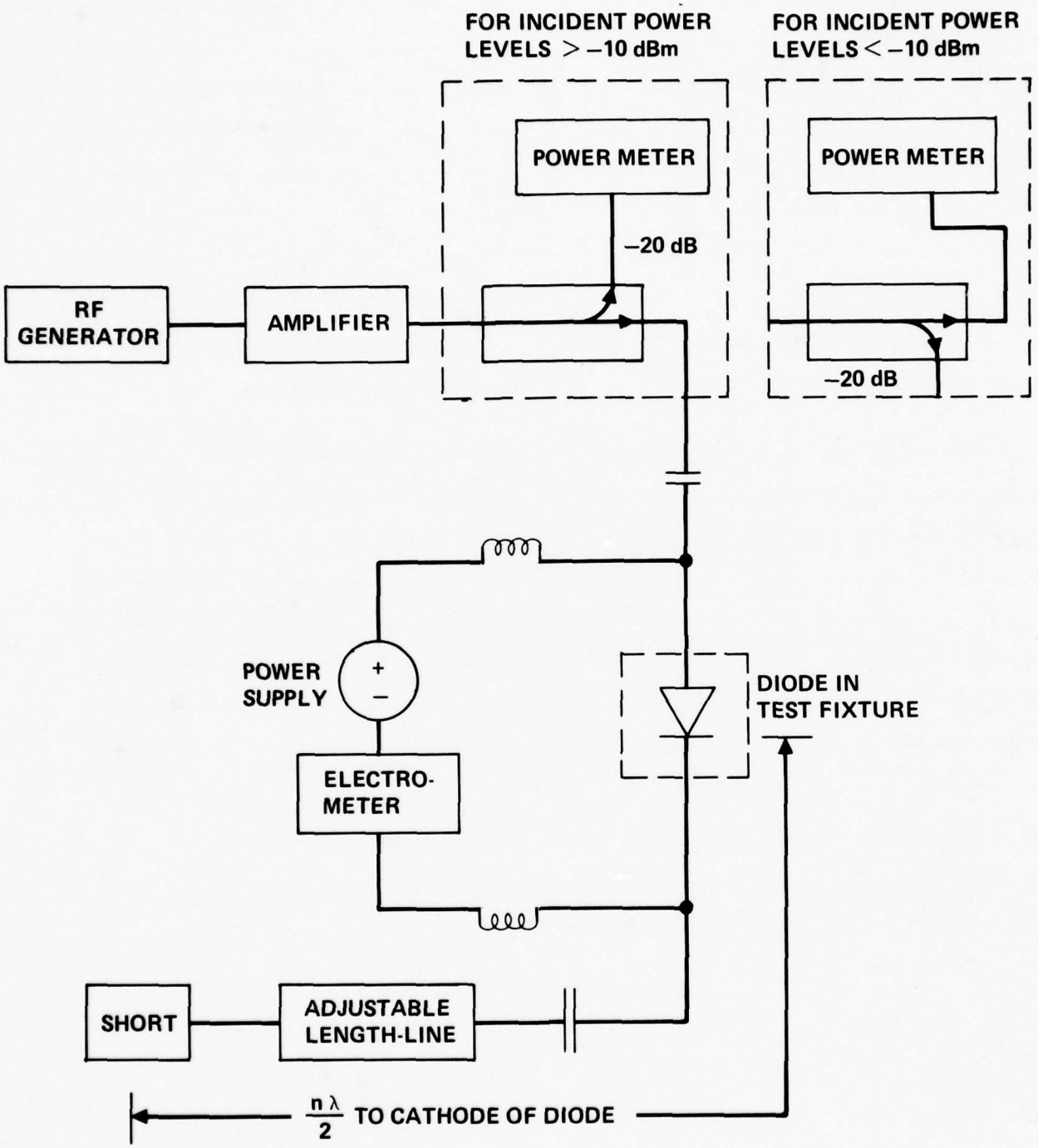


Figure 4.1. Typical Test Setup to Measure Current Rectification in Diodes

Figure 4.2 shows the rectification efficiency measured for a 1N718 diode versus bias voltage, frequency, and RF power level. For low RF power levels, the rectification efficiency remains constant with RF power and depends only on bias

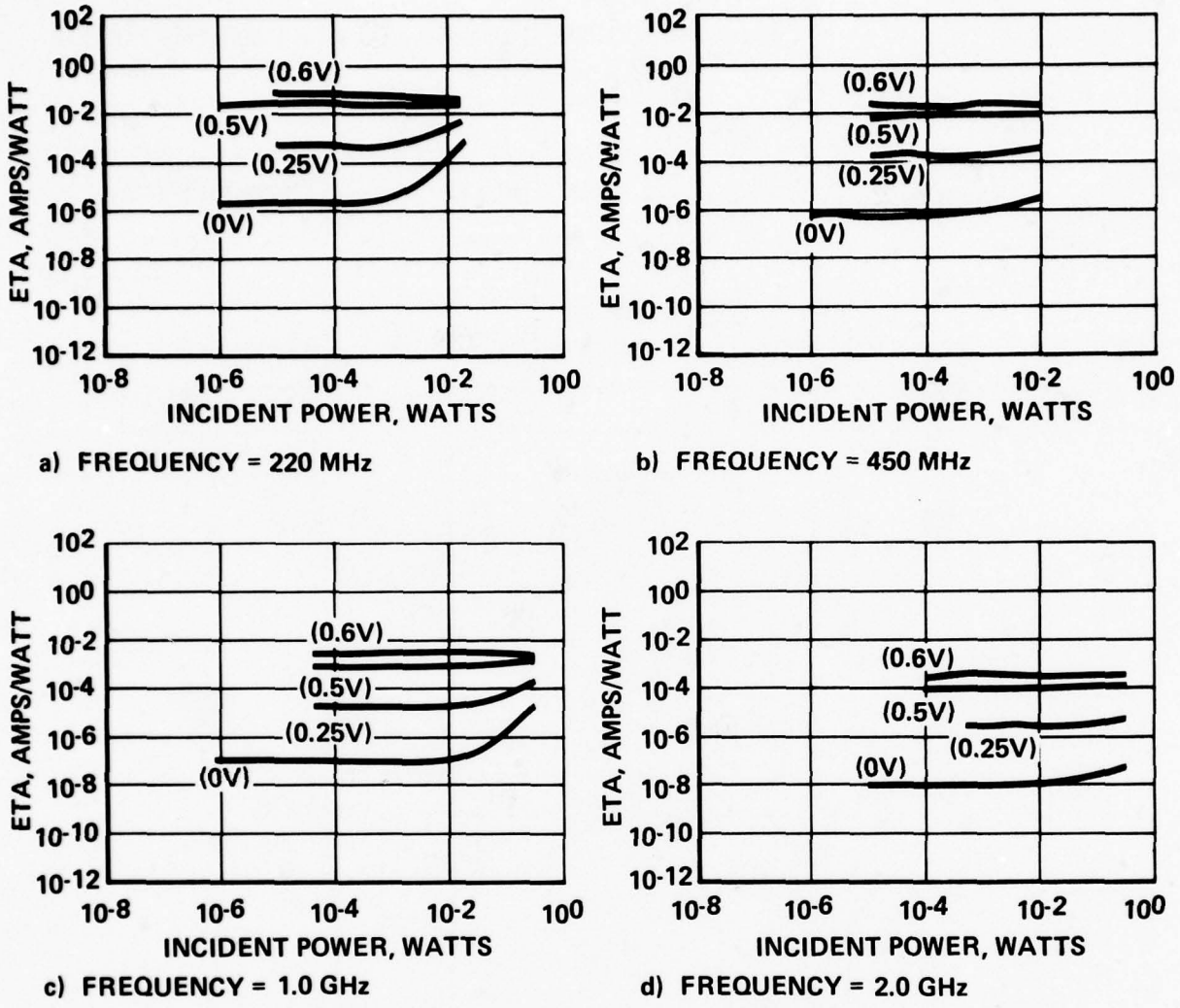


Figure 4.2. Rectification Efficiency Measured for 1N718 Diode versus Frequency, Bias Voltage, and RF Power Level.

voltage and frequency. This is the small signal (square law) region. At higher power levels, the rectification efficiency becomes greatly dependent on RF power level, as the rectification becomes a large signal phenomenon. With increasing frequency, the rectification efficiency decreases. For the 1N718, rectification efficiency decreases by an order of magnitude between frequencies of 1 GHz and 2 GHz. Also, the diode rectification obeys a square law dependence over a wider range of power as the frequency increases. For the 1N718, the square law region

includes RF powers less than approximately 10^{-4} watt at 220 MHz, but extends to 10^{-2} watt at 2 GHz.

Figure 4.3 shows the rectification efficiency measured for a 1N965B diode.

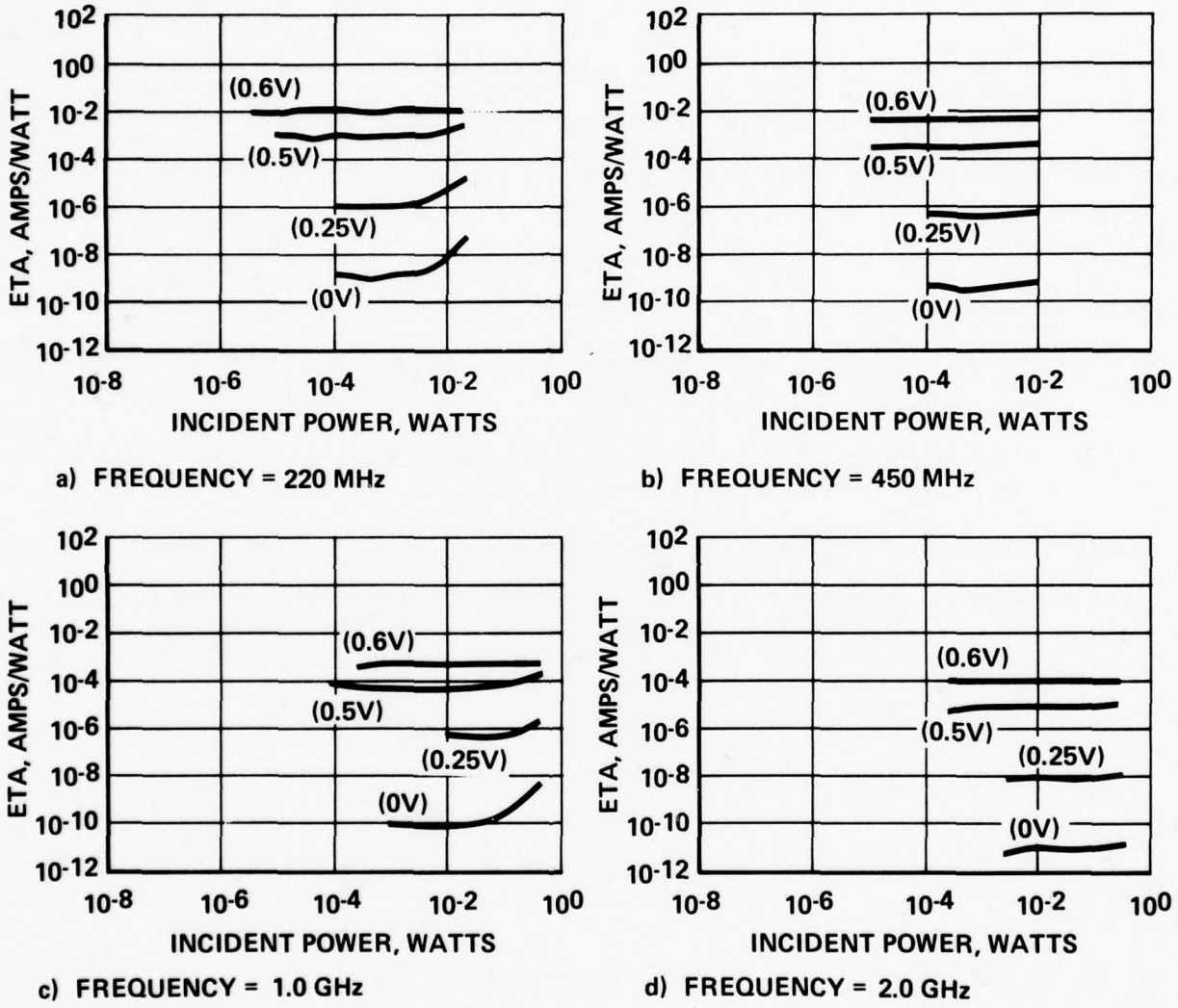


Figure 4.3. Rectification Efficiency Measured for 1N965B Diode versus Frequency, Bias Voltage, and RF Power Level.

These curves are similar in shape to those shown in Figure 4.2 for the 1N718. As with the 1N718, the 1N965B does not enter the large signal region at the power levels that were used in the testing. It is interesting to note the very large range over which the rectification efficiency varies with bias voltage: for bias

voltages between 0 and 0.60 volts, the rectification efficiency varies by a factor of 10^7.

Figure 4.4 shows the rectification efficiency measured for a 1N914 diode.

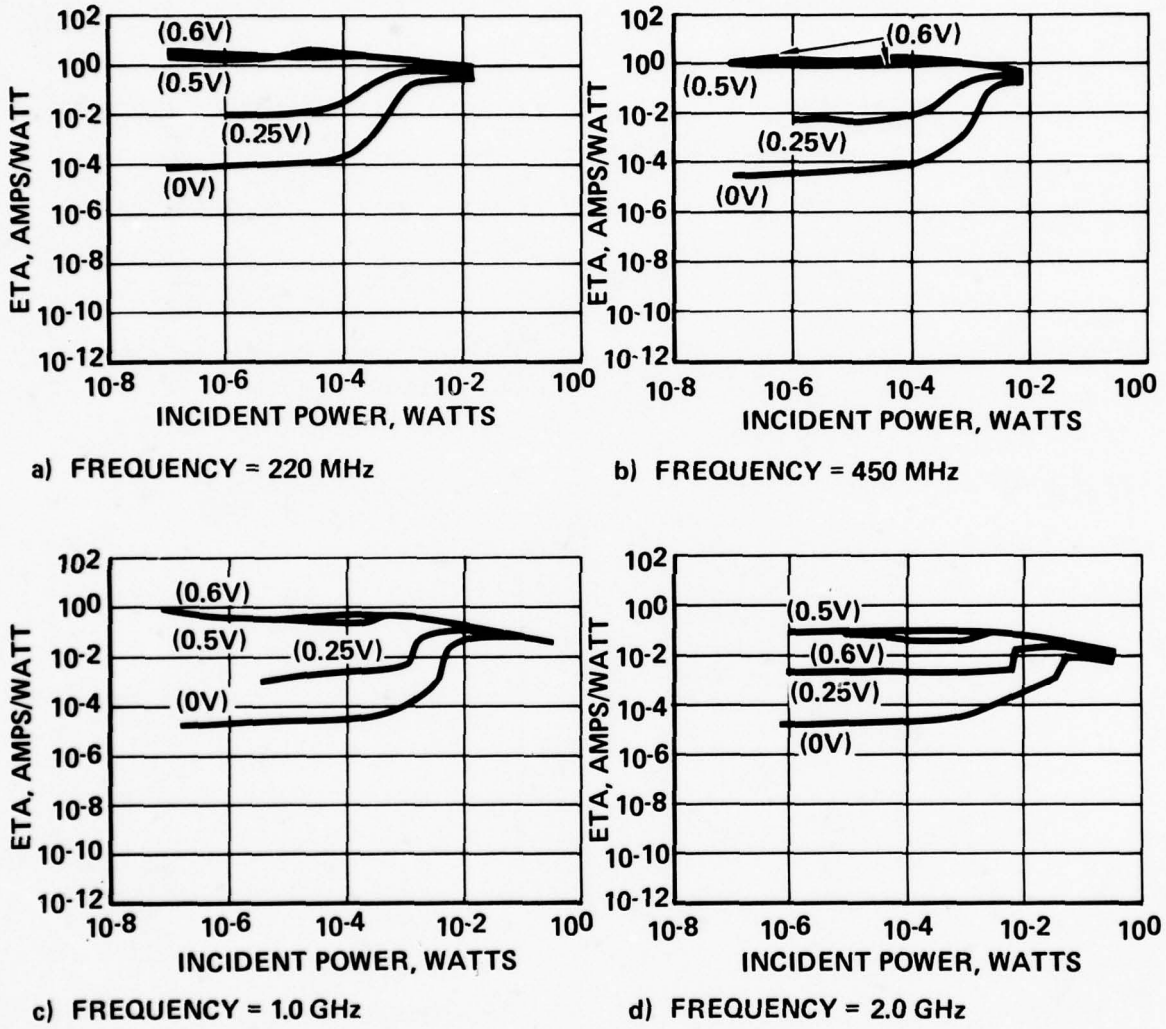


Figure 4.4. Rectification Efficiency Measured for 1N914 Diode Versus Frequency, Bias Voltage, and RF Power Level.

These curves are similar in shape to those shown in Figures 4.2 and 4.3. However, the 1N914 shows more clearly the large signal rectification region which occurs at the higher RF power levels. In this region, the rectification efficiencies for different bias voltages approach each other asymptotically (on a log plot) and

become proportional to $(P_{RF})^{-1/2}$. The rectified current is then proportional to $(P_{RF})^{1/2}$, which is the relation used in large signal interference models of diodes and bipolar transistors[1]. At a bias voltage of 0.5 or 0.6 volts, the 1N914 is in the large signal region at RF powers greater than 1 mW at a frequency of 220 MHz, and at RF powers greater than 4 mW at 1 GHz.

An unusual phenomenon occurs at 1 GHz and 2 GHz for the 1N914 diode that was not observed to occur with the other diodes. The rectification efficiency appears discontinuous at certain values of RF power. At 2 GHz, a discontinuity occurred at approximately 5 mW at a bias of 0.25 volts, and at approximately 40 mW at a bias of 0 volts. These discontinuities appeared to have a hystersis effect: the discontinuities occurred at different power levels depending on whether the RF power was being increased or decreased through the region. Closer examination of the rectification characteristics of this diode yield some insight into the cause of these discontinuities.

Figure 4.5 shows the IV characteristics measured for the 1N914 diode at a frequency of 2 GHz for power levels of 4.5 mW (6.56 dBm), 5.1 mW (7.06 dBm), and 5.7 mW (7.56 dBm). These curves show that a negative resistance region exists in the 1N914 diode characteristic. References [2] and [3] describe similar observations for germanium rectifiers. The reason that the negative resistance region occurs is not entirely clear. Torrey and Whitmer, in Reference [2], show that sufficient conditions for a negative resistance region to occur are: 1) the diode is representable by a nonlinear resistance in shunt with a voltage variable capacitance, 2) the spreading resistance of the diode must be small, and 3) the constant component of shunt capacitance must be small. However, they also conclude that the diode series inductance has some influence on the appearance of the negative resistance region.

An analytical approach to studying rectification using a Fourier expansion

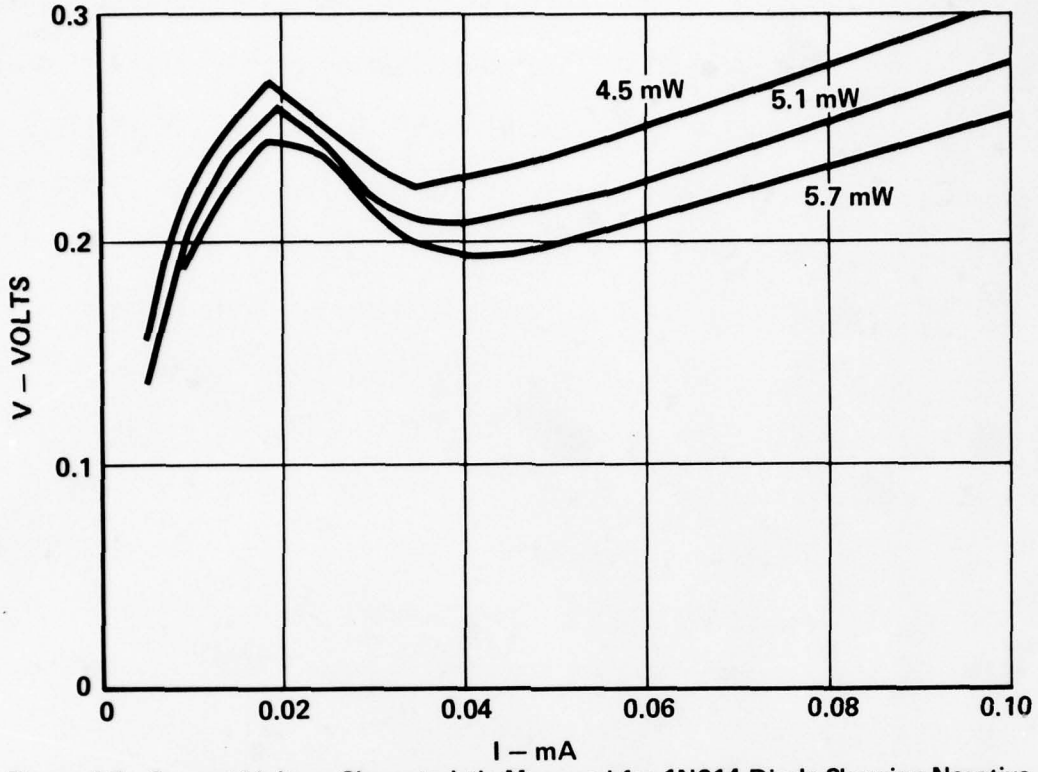


Figure 4.5. Current-Voltage Characteristic Measured for *1N914 Diode Showing Negative* Resistance Region Which Occurs When RF is Conducted into Diode at 2 GHz.

technique is described in the next section. The method predicts curves of similar shape versus RF power as those shown in Figures 4.2 through 4.4, and appears to be a fairly good representation of the rectification phenomenon because it encompasses both the large and small signal regions. (However, as presently formulated, the method does not predict the existence of a negative resistance region in the IC characteristics).

4.2 Rectification Theory Using Fourier Analysis

Earlier studies[4] have shown that rectification in a diode can be calculated by a time domain method: the junction current and voltage waveforms are calculated, then averaged over a period to obtain their dc values. This method is very time consuming, requiring the solution of nonlinear differential equations if diode capacitance is included. Small signal calculations are convenient, but can be used

only where RF power levels are quite small. A Fourier expansion method is much more convenient than the time domain method and is applicable over a wider range of power levels than the small signal approach. The theory is presented in this section.

Figure 4.6 illustrates a simple circuit for the study of diode rectification.

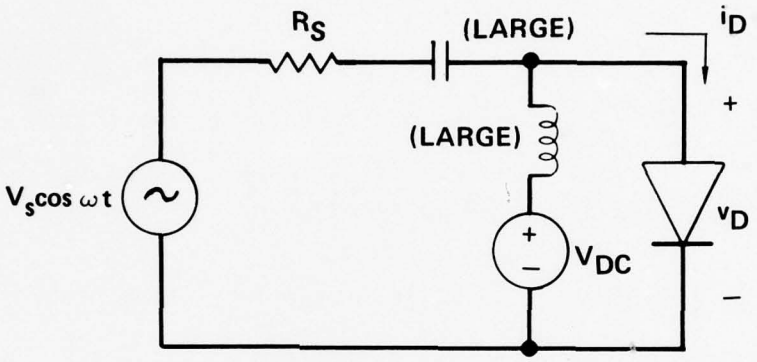


Figure 4.6. Circuit for Study of Diode Rectification

The relationship between the diode current, i_D, and the diode voltage, v_D, is

$$i_D = I_{DS}(e^{Qv_D} - 1), \tag{4.2}$$

where I_{DS} is the diode reverse saturation current, and Q is a constant having dimension $(\text{volts})^{-1}$. The RF source is assumed to contain a series resistance, R_S.

The diode current and voltage can be written in terms of their harmonic components:

$$i_D = I_{DC} + I_1 \cos \omega t + I_2 \cos 2\omega t + I_3 \cos 3\omega t + \ldots, \tag{4.3}$$

and

$$v_D = V_{DC} + (V_s - I_1 R_S) \cos \omega t - I_2 R_S \cos 2\omega t - I_3 R_S \cos 3\omega t - \ldots \tag{4.4}$$

(The inductor is assumed large so that is passes only dc current, and the capacitor is assumed large so that it passes all ac components of current). Substitute for v_D in equation (4.2) to obtain

$$i_D = I_{DS}(e^{Qv_{DC}} e^{Q(V_s - I_1 R_S) \cos \omega t - QI_2 R_S \cos 2\omega t \ldots} - I_{DS}.$$

Define:

$$X_1 = Q(V_s - I_1 R_S)$$

$$X_2 = -QI_2 R_S$$

$$X_3 = -QI_3 R_S, \text{ etc.}$$

Then the diode current can be written

$$i_D = I_{DS} e^{QV_{DC}} (e^{X_1 \cos \omega t} e^{X_2 \cos 2\omega t} e^{X_3 \cos 3\omega t} \ldots) - I_{DS}. \qquad (4.5)$$

The quantity $e^{X\cos \omega t}$ can be expanded in terms of its Fourier components:

$$e^{X\cos\omega t} = [I_o(X) + 2 \sum_{n=1}^{\infty} I_n(X) \cos n\omega t],$$

where $I_n(X)$ is a modified Bessel function of the first kind of order n and argument X. The diode current can then be written

$$\begin{aligned} i_D = -I_{DS} + I_{DS} e^{QV_{DC}} & [I_o(X_1) + 2 \sum_{n=1}^{\infty} I_n(X_1) \cos n\omega t] \\ & \cdot [I_o(X_2) + 2 \sum_{n=1}^{\infty} I_n(X_2) \cos 2n\omega t] \\ & \cdot [I_o(X_3) + 2 \sum_{n=1}^{\infty} I_n(X_3) \cos 3n\omega t] \\ & \cdot \text{ etc.} \end{aligned} \qquad (4.6)$$

As a simplification, assume that the higher harmonic components of current and voltage are small, i.e., that X_2, X_3, X_4, etc. are small, then

$$1 \simeq I_o(X_2) \simeq I_o(X_3) \simeq I_o(X_4) \simeq \cdots$$

and

$$0 \simeq I_n(X_2) \simeq I_n(X_3) \simeq I_n(X_4) \simeq \cdots,$$

for all $n > 0$. Then equation (4.6) simplifies to

$$i_D = -I_{DS} + I_{DS} e^{QV_{DC}} [I_o(X_1) + 2 \sum_{n=1}^{\infty} I_n(X_1) \cos n\omega t]. \qquad (4.7)$$

By comparing (4.7) with (4.3), it is apparent that

$$I_{DC} = -I_{DS} + I_{DS} e^{QV_{DC}} I_o(X_1)$$

and

$$I_1 = I_{DS} e^{QV_{DC}} 2I_1(X_1).$$

The functions $I_o(X)$ and $I_1(X)$ can be written as series expansions:

$$I_o(X) = 1 + \frac{X^2}{2^2} + \frac{X^4}{2^2 \cdot 4^2} + \frac{X^6}{2^2 \cdot 4^2 \cdot 6^2} + \ldots \quad (4.8)$$

$$I_1(X) = \frac{X}{2} + \frac{X^3}{2^2 \cdot 4} + \frac{X^5}{2^2 \cdot 4^2 \cdot 6} + \ldots \quad (4.9)$$

The result is three equations in three unknowns (I_{DC}, I_1, X_1):

$$I_{DC} = -I_{DS} + I_{DS} e^{QV_{DC}} I_o(X_1) \quad (4.10)$$

$$I_1 = 2I_{DS} e^{QV_{DC}} I_1(X_1) \quad (4.11)$$

$$X_1 = Q(V_s - I_1 R_S). \quad (4.12)$$

These equations can be solved numerically (using equations (4.8) and (4.9)) to find the dc current that results for a given RF source amplitude, V_s.

Figure 4.7 shows the I_{DC} vs. V_{DC} curves which are predicted by equations (4.10) - (4.12). The diode was assumed to have $I_{DS} = 1 \times 10^{-14}$ amps and Q = 1/(.026 volt), and the RF source resistance was 50Ω. The shape of the curves is similar to those measured in the lab and predicted by time domain calculations.

Figure 4.8 compares an I_{DC} vs. V_{DC} curve calculated by the Fourier expansion method with one calculated with the time domain method. The Fourier method predicts a curve that is a fairly good representation of that predicted by the more accurate time domain method. The difference between the curves is due to the simplifying assumptions. Greater accuracy can be obtained by including the next several harmonic components in the calculations, but this would increase the difficulty of solution. Figure 4.8 illustrates that good accuracy can be obtained by solving equations (4.10) - (4.12), with much less effort that is required with a time domain calculation.

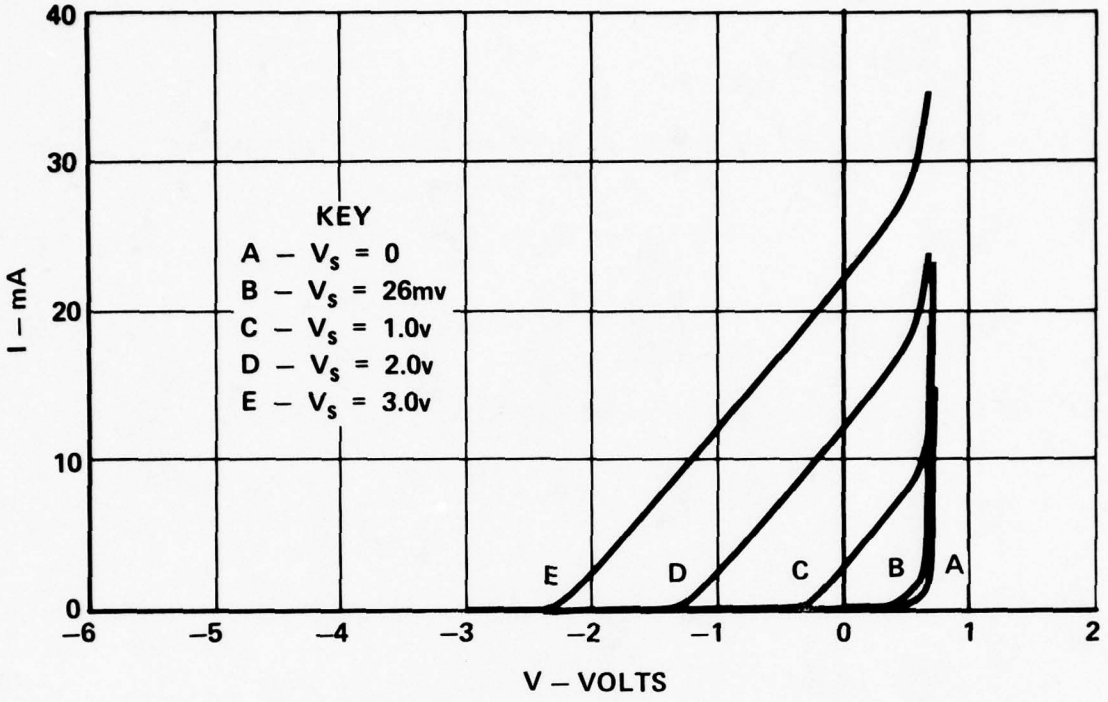


Figure 4.7 Predicted Diode Rectification Using Fourier Expansion Method

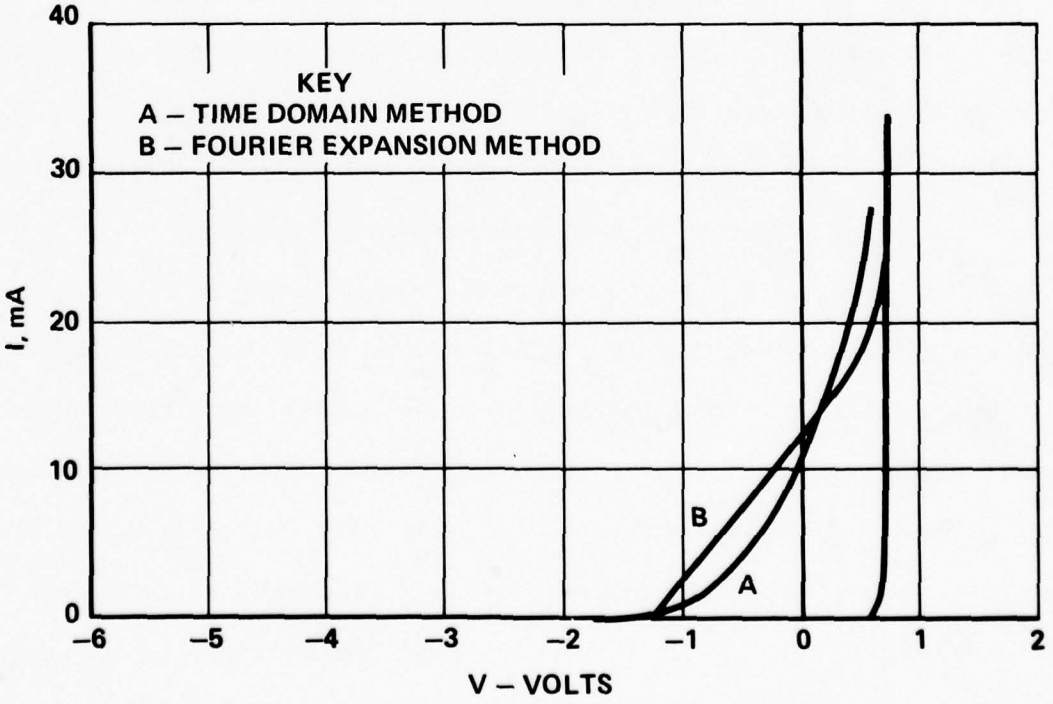


Figure 4.8. Comparison of Methods for Predicting Junction Rectification

This method can be applied to the more general circuit shown in Figure 4.9.

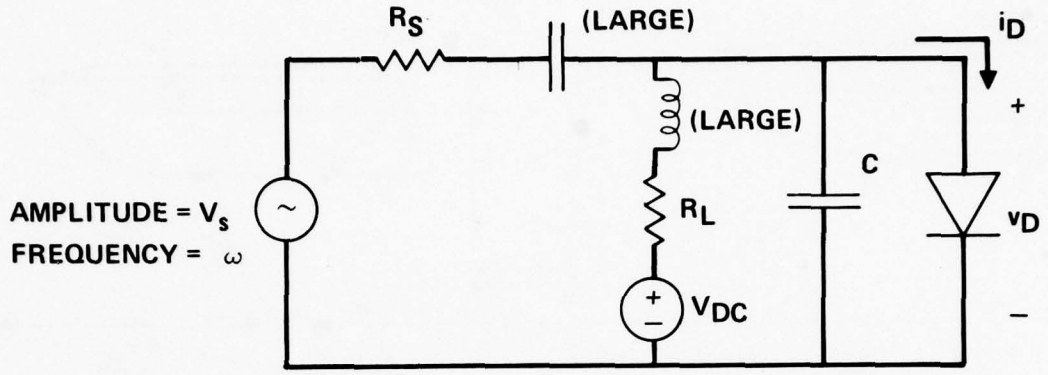


Figure 4.9. General Circuit for Study of Diode Rectification

Here, the diode capacitance is represented as the sum of a constant capacitance term, C_o, and a voltage-variable term:

$$C = C_o + KI_{DS}e^{QV_D}, \tag{4.13}$$

where K is a constant with units farads/amp.

The development is similar to the earlier case and, as before, the higher harmonic components are assumed small. The result is 4 equations in 4 unknowns:

$$I_{DC} = -I_{DS} + I_{DS}e^{QV_D}I_o(X_1) \tag{4.14}$$

$$X_1 = QV_1 \tag{4.15}$$

$$V_S^2 = [V_1 + 2R_SI_{DS}e^{QV_D}I_1(X_1)]^2 + [\omega V_1R_S(C_o + 2KI_{DS}e^{QV_D}I_1(X_1)/X_1)]^2 \tag{4.16}$$

$$V_D = V_{DC} - I_{DC}R_L. \tag{4.17}$$

In this case, the dc component of voltage across the diode is V_D, and V_{DC} is the dc supply voltage. These equations can be solved numerically to yield the dc components of current and voltage resulting from the RF signal.

Predictions were made of the rectification efficiencies of several diodes. Figures 4.10 and 4.11 show the rectification efficiencies that were predicted for types 1N718 and 1N965B diodes, respectively. The parameters used in the calculations were measured in the laboratory for particular diodes, and are listed

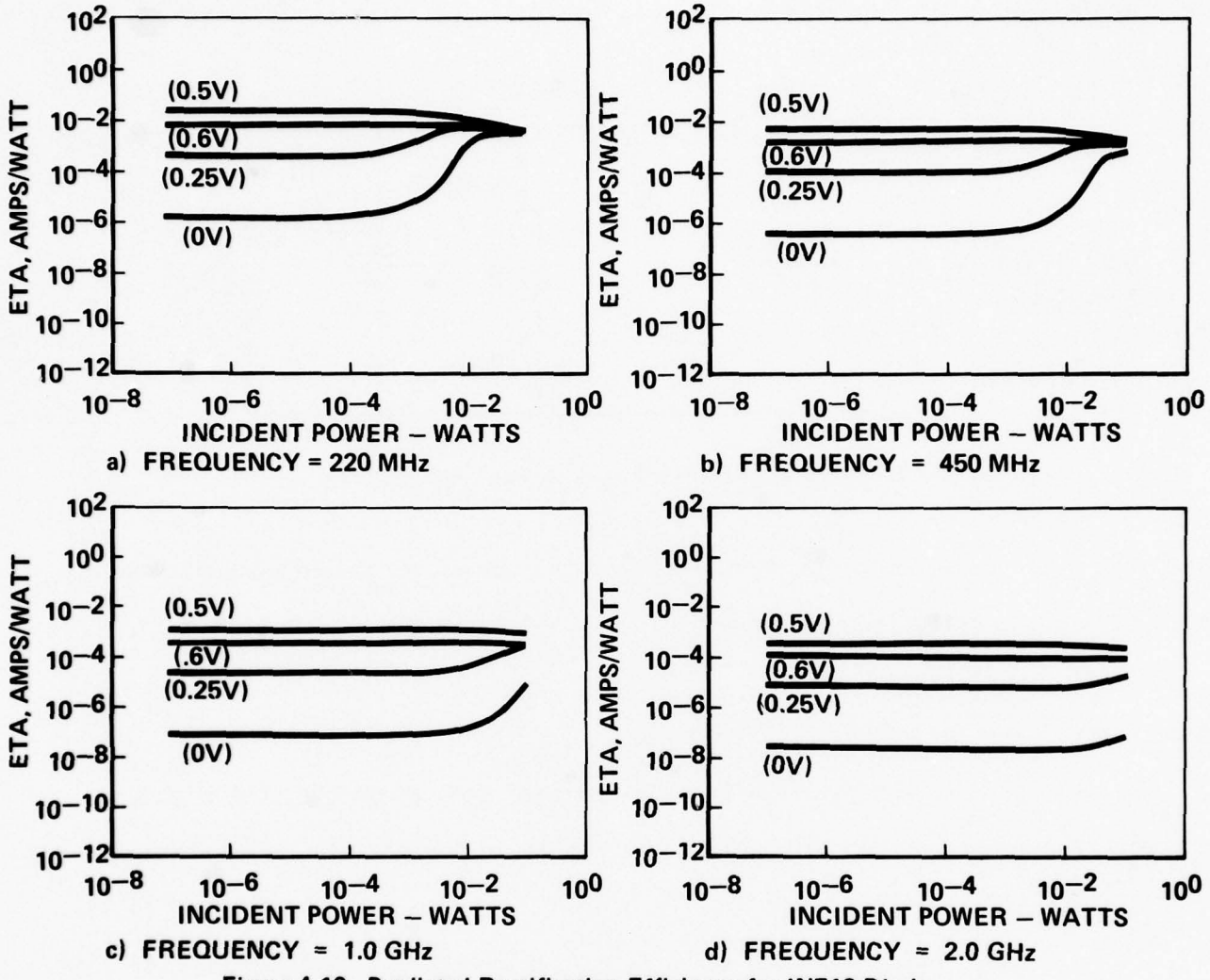
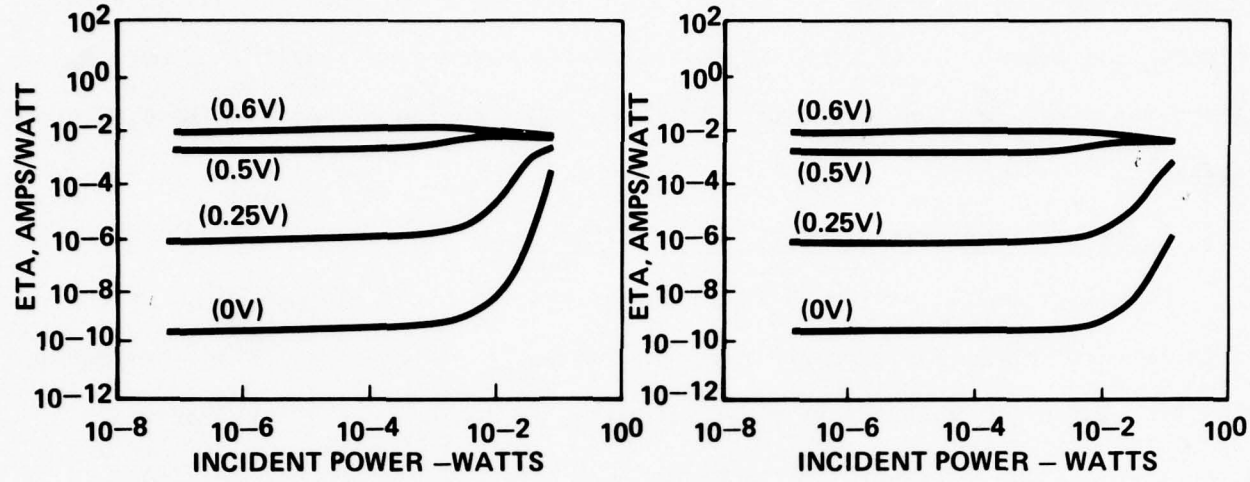


Figure 4.10. Predicted Rectification Efficiency for IN718 Diode

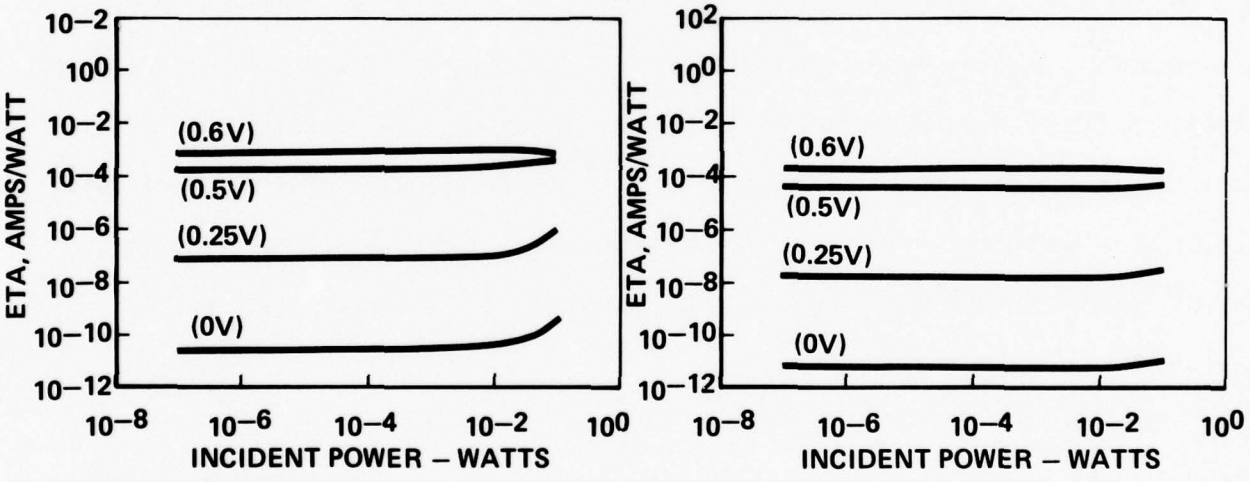
in Table 4.1. The incident RF power level, P_{RF}, was given by $P_{RF} = V_S^2/400\Omega$. The diode was assumed biased with a voltage source, so $R_L = 0$.

Comparison of Figures 4.10 and 4.11 with the measured data in Figures 4.2 and 4.3 shows the method to be fairly accurate in predicting the wide variations in rectification efficiency that occur with bias voltage and power level. In the IN718 data the rectification efficiency of the $V_{DC} = .6$ volt case was measured to be higher (by a factor of 10) than predicted. Also, the power levels where the rectification efficiency enters the large signal regime vary somewhat (about



a) FREQUENCY = 220 MHz

b) FREQUENCY = 450 MHz



c) FREQUENCY = 1.0 GHz

d) FREQUENCY = 2.0 GHz

Figure 4.11. Predicted Rectification Efficiency for IN965B Diode

Table 4.1. Diode Parameters for Rectification Efficiency Calculations

	IN718	IN965B
Q (VOLTS^{-1})	22.45	31.14
I_{DS} (AMPS)	3.63×10^{-10}	2.82×10^{-13}
K (FARADS/AMP)	2.289×10^{-6}	3.215×10^{-6}
C_D (pF)	47.3	97.0

3 dB) between the predicted and measured curves. This may occur because, in this region, the assumption of small higher harmonics may become invalid. A more elaborate model, including series resistance and inductance, may give more accurate results.

4.3 Worst Case Analysis of Junction Rectification

Models of rectification in PN junctions are the basic elements from which interference models for complete circuits are built. A model which approximates the RF induced IV characteristics of the diode in a piecewise linear manner is described in this section. The model is much simpler than the one described in the previous section, and is similar to the diode rectification model described in the Handbook[1] and used in models of interference in TTL devices and op amps. The model parameters depend on the electrical properties of the diode itself, and those of the RF driving source as seen from the diode. In general, the RF driving impedance will be an unknown complex quantity. When evaluating circuit responses through an interference simulation, the effect of all possible values of RF impedance must be considered, and the most detrimental circuit response should be found.

A model of a diode driven by an RF Thevenin source is shown in Figure 4.12. The diode is represented by an ideal diode with a parallel capacitance, C (assumed constant), and series resistance r_S. The capacitor represents the junction capacitance and any parasitic capacitance which shunts the diode junction. Resistor r_S includes lossy elements within the diode itself, such as bulk resistance, and those external to the diode, such as the losses associated with cables, printed circuit wiring, etc. The RF Thevenin source is represented by a voltage generator $V_s \sin \omega t$ of frequency $\frac{\omega}{2\pi}$ and amplitude V_s (peak voltage, not RMS) with series impedance $R_S + jX_S$. The dc bias voltage for the diode is supplied by voltage source V_0. A large capacitor and inductor form a biasing

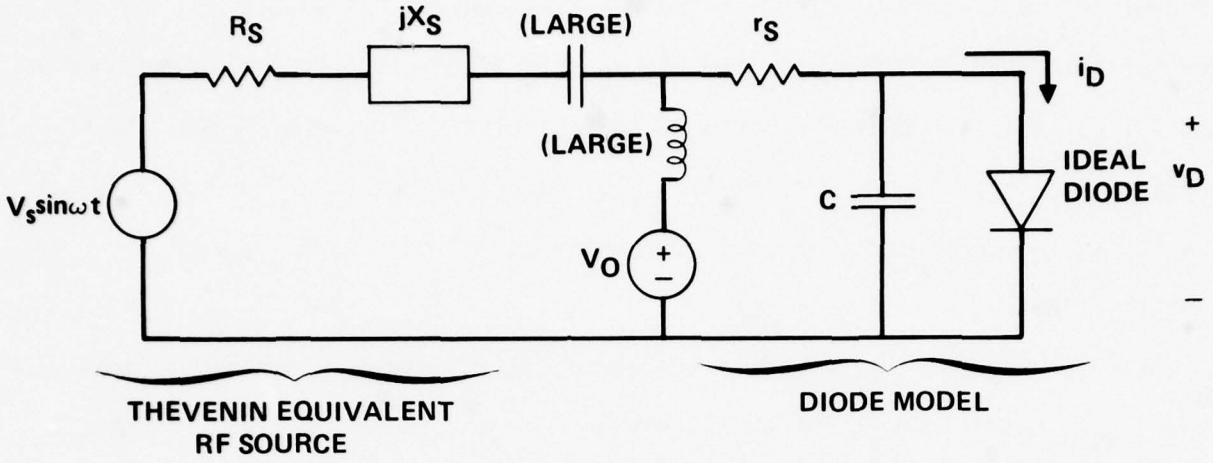


Figure 4.12. Circuit for Study of Diode Rectification Response Due to Arbitrary RF Source.

arrangement to allow superposition of the dc and RF signals.

Figure 4.13 shows the RF induced IV characteristics which result for the

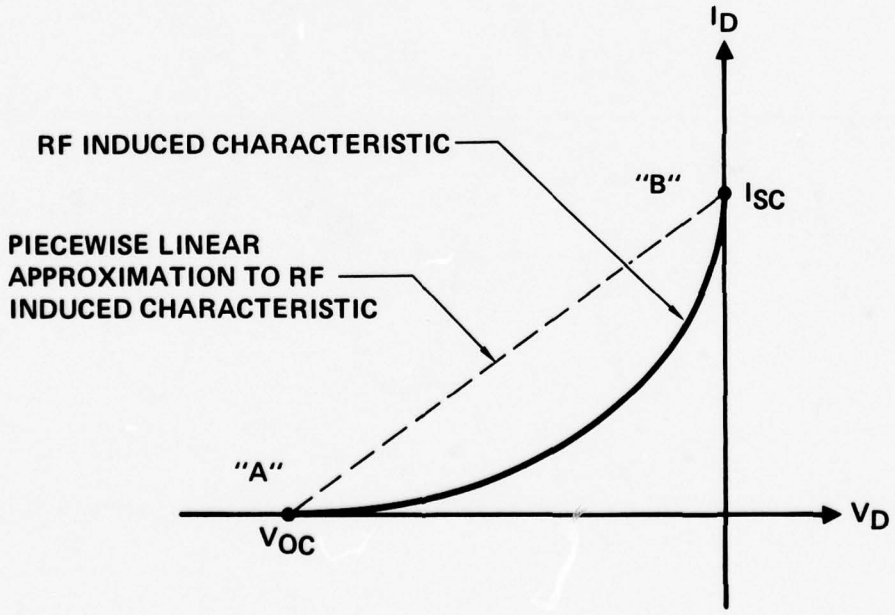


Figure 4.13. Typical RF Induced IV Characteristic for a Diode Showing Piecewise Linear Approximation Used in Rectification Model.

ideal diode in the circuit shown in Figure 4.12. The solid line shows the shape of a typical RF induced characteristic; the dashed line shows a piecewise

approximation to the curve which is linear between points "A" and "B" on the IV characteristic. Point "A" has $I_D = 0$ and $V_D = V_{OC}$, where V_{OC} is the largest value of V_D for which $I_D = 0$ on the RF induced characteristic. (V_D and I_D are time-averaged values of v_D and i_D, respectively). Point "B" has $V_D = 0$ and $I_D = I_{SC}$, where I_{SC} is the smallest value of I_D for which $V_D = 0$ on the RF induced characteristic.

The determination of the rectified current is in general a nonlinear problem, however the problem becomes linear at voltages $V_D \leq V_{OC}$ and at currents $I_D \geq I_{SC}$. At point "A" in Figure 4.13, the ideal diode remains off for all time, and the resulting ideal diode voltage waveform is as shown in Figure 4.14. The highest

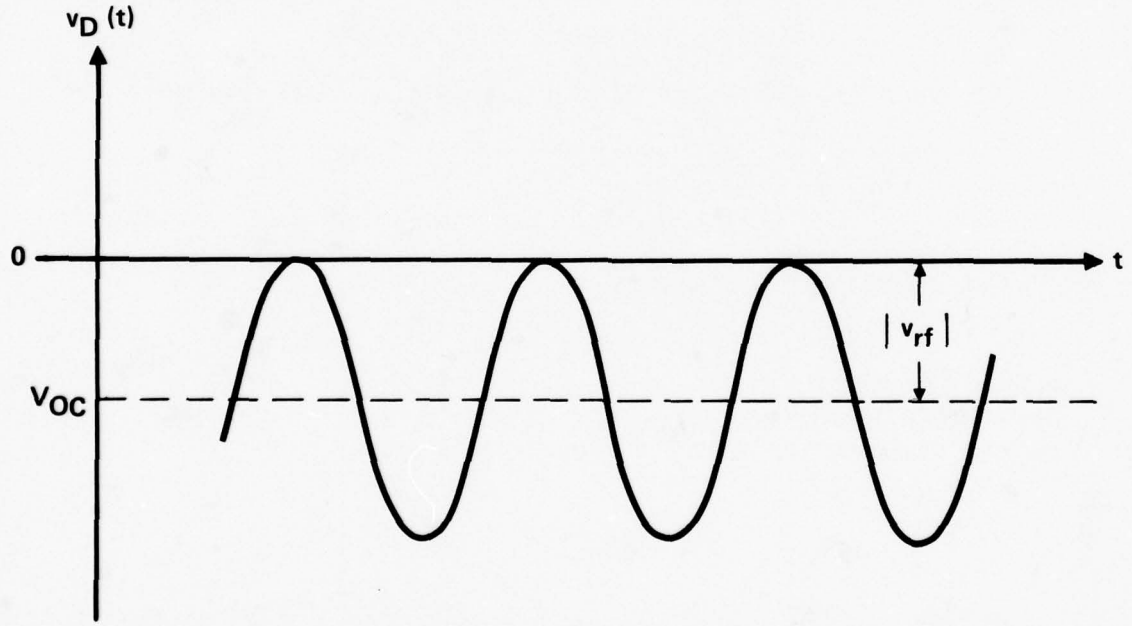


Figure 4.14. Ideal Diode Voltage Waveform When Biased at $V_D = V_{OC}$ and $I_D = 0$. (Point A in Figure 2).

voltage reached by the waveform is $v_D = 0$, the point at which the diode begins to conduct. The ac component of the voltage is sinusoidal, and the dc component (or average value) of the waveform, V_{OC}, is the negative of the magnitude of the ac voltage. The ac voltage across the diode can be determined from the circuit

shown in Figure 4.15. In this circuit the ideal diode is replaced with an open circuit, and the ac voltage across the ideal diode, v_{rf}, can be found. The magnitude of the open circuit voltage is then

$$V_{OC} = -|v_{rf}| = -V_s/[(1 - \omega C X_S)^2 + (\omega C)^2 (R_S + r_S)^2]^{1/2} \qquad (4.18)$$

At point "B" in Figure 4.13, the ideal diode is on for all time. The resulting diode current waveform is shown in Figure 4.16. The lowest current

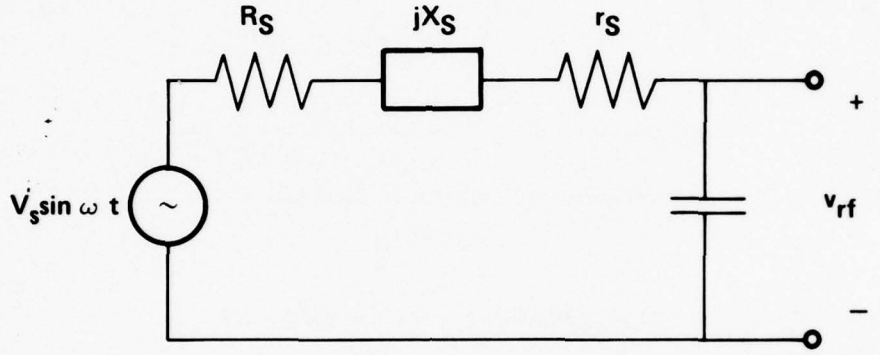


Figure 4.15. Circuit to Find V_{OC}. ($V_{OC} = |v_{rf}|$)

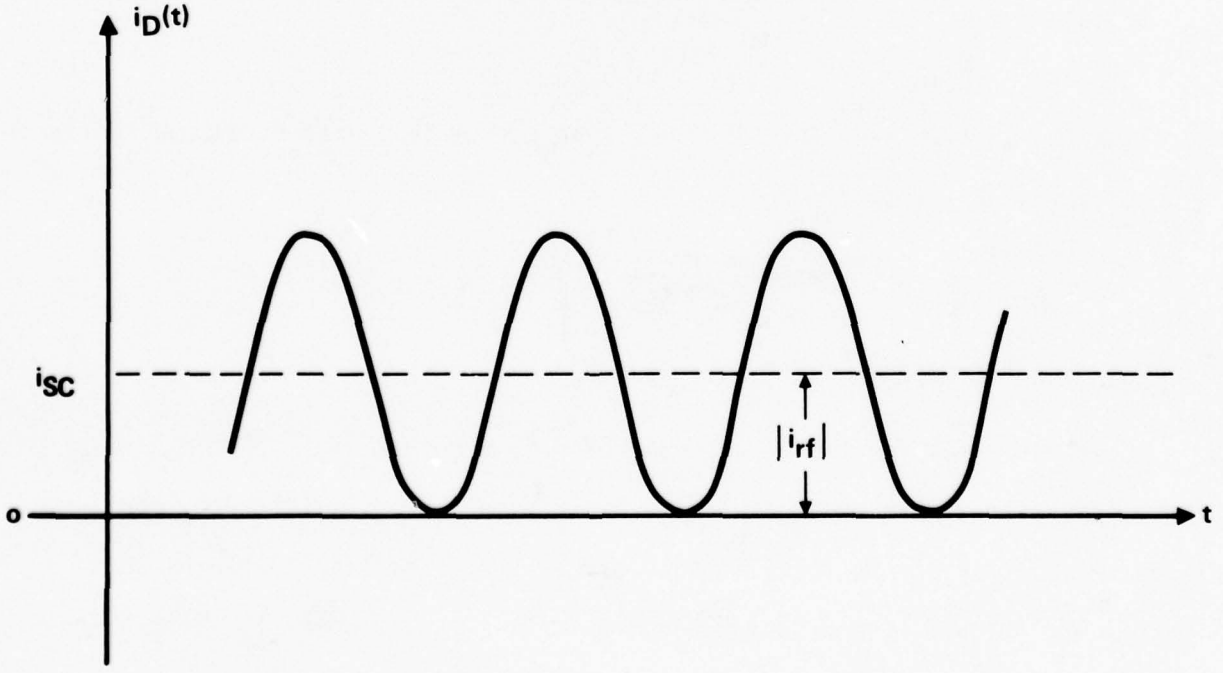


Figure 4.16. Ideal Diode Current Waveform When Biased at $V_D = 0$ and $I_D = I_{SC}$. (Point B in Figure 2)

reached is $i_D = 0$. Once again, the ac component of the waveform is sinusoidal and can be found through a linear analysis by replacing the ideal diode with a short circuit as shown in Figure 4.17. The value of I_{SC} equals the magnitude of

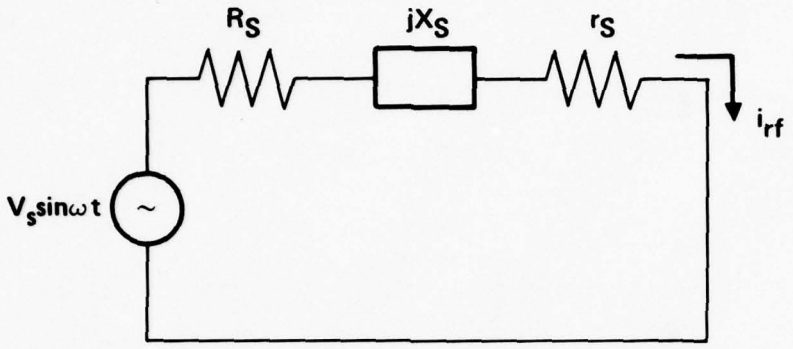


Figure 4.17. Circuit to Find I_{SC}. ($I_{SC} = |i_{rf}|$)

the ac component of the current waveform. It is given by

$$I_{SC} = |i_{rf}| = V_s/[(R_S + r_S)^2 + X_S^2]^{1/2}. \tag{4.19}$$

If we use

$$P_{RF} = V_s^2/8R_S \tag{4.20}$$

to relate the maximum available RF power that can be delivered to a load to the value of V_S and R_S, then V_{OC} and I_{SC} become

$$V_{OC} = (8P_{RF}R_S)^{1/2}/[(1 - \omega CX_S)^2 + (\omega C)^2 (R_S + r_s)^2]^{1/2} \tag{4.21}$$

$$I_{SC} = (8P_{RF}R_S)^{1/2}/[(R_S + r_s)^2 + X_S^2]^{1/2}. \tag{4.22}$$

A circuit model for the diode considered in Figure 4.12, including the effects of rectification, is shown in Figure 4.18. Elements D1, D2, I_X and R_X model the piecewise behavior of the rectification occurring in the ideal diode as shown in Figure 4.13. Diodes D1 and D2 are assumed ideal. The value of I_X is I_{SC}, and

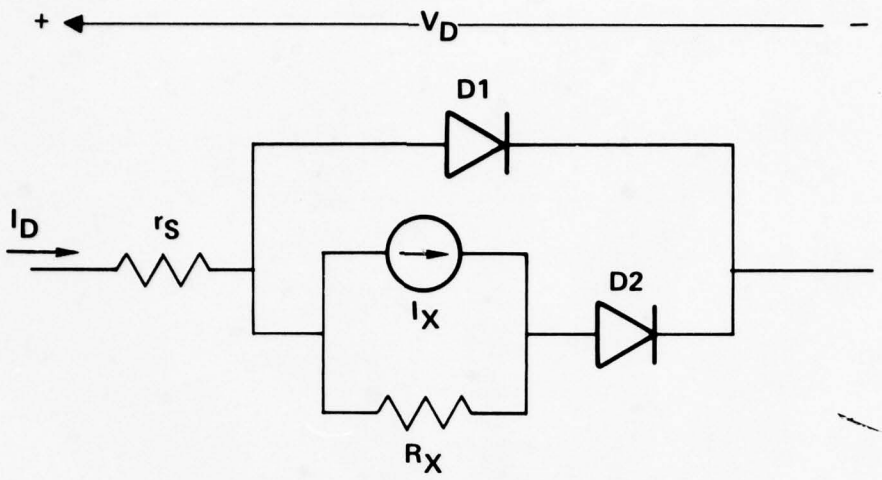


Figure 4.18. Diode Rectification Model.

can be expressed as

$$I_X = KP_{RF}^{1/2} \tag{4.23}$$

where

$$K = (8R_S)^{1/2}/[(R_S + r_S)^2 + X_S^2]^{1/2} \tag{4.24}$$

The value of R_X is V_{OC}/I_{SC}, which gives

$$R_X = [(R_S + r_s)^2 + X_S^2]^{1/2}/[(1 - \omega CX_S)^2 + (\omega C)^2 (R_S + r_s)^2]^{1/2}. \tag{4.25}$$

Series resistances r_S in Figures 4.12 and 4.18 are the same.

It is convenient at this point to normalize K and R_X with respect to $1/\omega C$. Normalized K (written $\hat{K}$) is defined by

$$\hat{K} \equiv K/(8\omega C)^{1/2} = (\hat{R}_S)^{1/2}/[(\hat{R}_S + \hat{r}_S)^2 + \hat{X}_S^2]^{1/2} \tag{4.26}$$

and normalized R_X (written $\hat{R}_X$) is

$$\hat{R}_X = \omega CR_X = [(\hat{R}_S + \hat{r}_S)^2 + \hat{X}_S^2]^{1/2}/[(1 - \hat{X}_S)^2 + (\hat{R}_S + \hat{r}_S)^2]^{1/2} \tag{4.27}$$

where normalized R_S, r_S and X_S are defined by

$$\hat{R}_S \equiv \omega CR_S$$

$$\hat{r}_S \equiv \omega Cr_S$$

$$\hat{X}_S \equiv \omega CX_S.$$

The normalization removes the frequency terms from the equations, simplifying later analysis.

In order to perform worst case analyses, it is desired to know the ranges of possible values of $\hat{R}_X$ and $\hat{K}$ for all possible values of $\hat{R}_S$ and $\hat{X}_S$. The minimum and maximum values of $\hat{R}_X$ can be shown to be

$$\hat{R}_{X_{min}} = 2\hat{r}_S/(1 + (1 + 4\hat{r}_S^2)^{1/2}) \tag{4.28}$$

$$\hat{R}_{X_{max}} = (1 + (1 + 4\hat{r}_S^2)^{1/2})/2\hat{r}_S. \tag{4.29}$$

Note that the minimum and maximum values of $\hat{R}_X$ are reciprocals. For small values of $\hat{r}_S$ (= $\omega C r_S$), and unnormalizing, we find

$$\lim_{\omega C r_S \to 0} \quad R_{X_{min}} = r_S \tag{4.30}$$

and

$$\lim_{\omega C R_S \to 0} \quad R_{X_{max}} = 1/(\omega C)^2 r_S. \tag{4.31}$$

At each value of $\hat{R}_X$ between $\hat{R}_{X_{min}}$ and $\hat{R}_{X_{max}}$, the maximum value of $\hat{K}$ is

$$\hat{K}_{max} = \frac{1}{\hat{R}_X} \left\{ \frac{\hat{R}_X(1 + \hat{R}_X^2) - \hat{r}_S\,(1 - \hat{R}_X^2)^2\,(1 + \hat{4}r_S^2)^{1/2}}{4\hat{R}_X\,\hat{r}_S + (1 + \hat{R}_X^2)\,(1 + 4\hat{r}_S^2)^{1/2}} \right\}^{1/2}. \tag{4.32}$$

Figure 4.19 illustrates the expected range of $\hat{K}$ and $\hat{R}_X$. Any values within the shaded region are possible, where the upper envelope of the shaded region is given by Equation (4.32). In this plot, the value of $\hat{r}_S$ is assumed to be 0.01, meaning $r_S = 1/100\omega C$. The shape of the plot is similar for different values of $\hat{r}_S$, but the range of $\hat{R}_X$ covered varied for different choices of $\hat{r}_S$, as given by Equations (4.28) and (4.29).

When analyzing worst case circuit response with this model, the envelope of the $\hat{K}$ versus $\hat{R}_X$ curve (given by Equation (4.32)), is expected to contain the

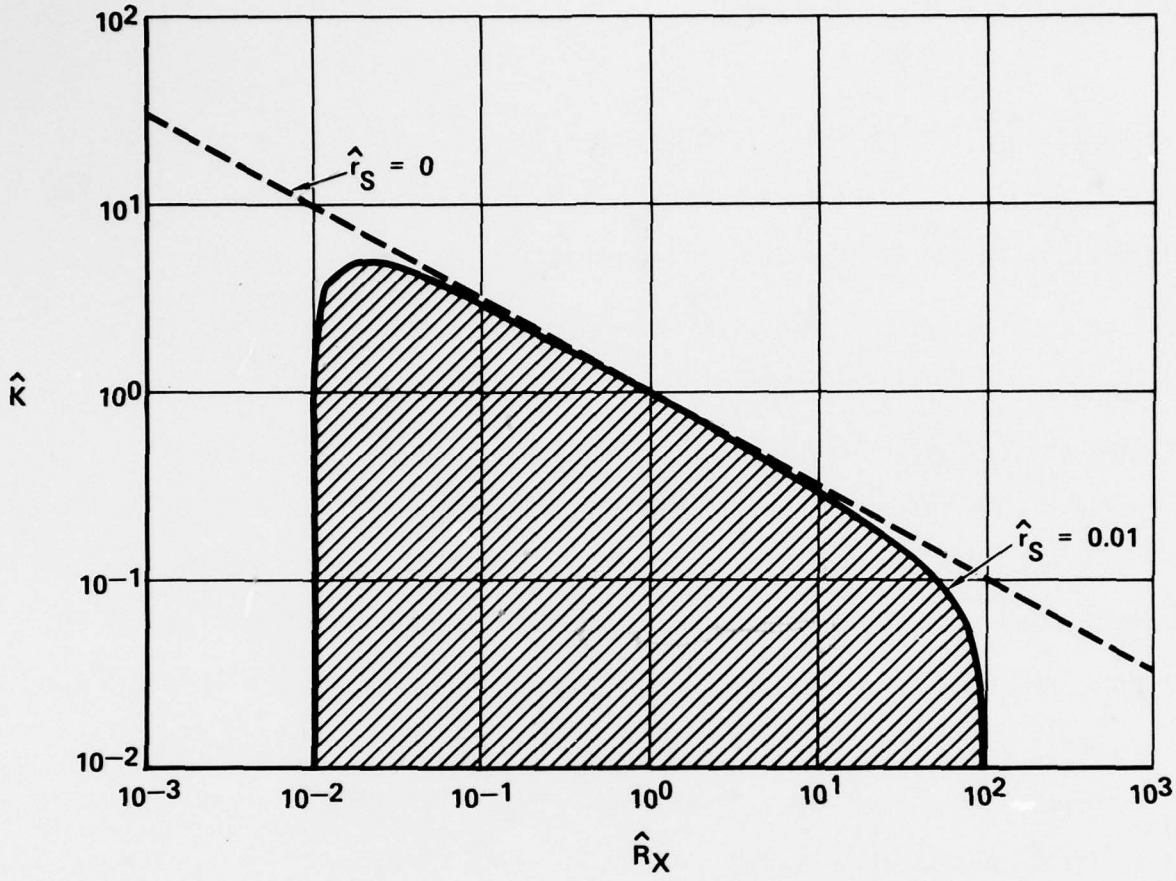


Figure 4.19. Expected Range of $\hat{K}$ and $\hat{R}_X$.

values of $\hat{K}$ and $\hat{R}_X$ that will give the worst case interference response. In order to find the worst case response for a circuit, values of $\hat{R}_X$ and $\hat{K}_{max}$ are chosen from Equations (4.28), (4.29) and (4.32), and the circuit response is calculated for each set of values. Sweeping $\hat{R}_X$ over its possible range, or use of iterative method are possible procedures to find the worst case interference response.

For the case of a diode with no loss ($r_S = 0$), Equation (4.32) gives

$$\hat{K}_{max} = (1/\hat{R}_X)^{1/2}$$

or in non-normalized values,

$$K_{max} = (8/R_X)^{1/2}. \qquad (4.33)$$

With no loss, the range of $\hat{R}_X$ is given by Equations (4.28) and (4.29) as

$$0 < \hat{R}_X < \infty \tag{4.34}$$

which means that the non-normalized R_X can assume any real positive value. Equation (4.33) is plotted as the dashed line in Figure 4.19. Clearly, the rectification in the no-loss case is greater than when loss is present in the diode, so the assumption of no loss is expected to yield a "worse" worst case response when interference analyses are performed.

4.4 Simulation of Interference in TTL NAND Gates

During this increment, the circuit analysis program SPICE (Simulation Program with Integrated Circuit Emphasis) was used to simulate interference effects in a 7400 NAND gate, a widely used TTL device. SPICE was developed specifically for analyzing integrated circuits under normal conditions when no interfering signals are present. It is commonly used by circuit designers, integrated circuit manufacturers, and universities. Reference [5] describes the program, its availability, and its input code.

Earlier investigations[6] showed the 7400 NAND gate is most susceptible to RF conducted into its output terminal when the output voltage is low (<0.4V), which occurs when both input voltages are high (>2.0V). RF signals conducted into the output terminal can cause the output voltage to change from a normal low state to a RF-induced high state. This is the situation that is simulated in this section.

A schematic diagram of a 7400 NAND gate with external connections is shown in Figure 4.20. The dual emitter transistor T1 was modeled by a single emitter transistor, and diodes D1 and D2 were modeled by a single diode DIN. Previous analysis had shown that when RF is injected into the 7400 NAND gate output with the output voltage low the interference effect can be described by assuming all of the RF power is incident on the output transistor[7]. Transistor T4 is modeled using the previously developed modified Ebers-Moll model[1], which includes

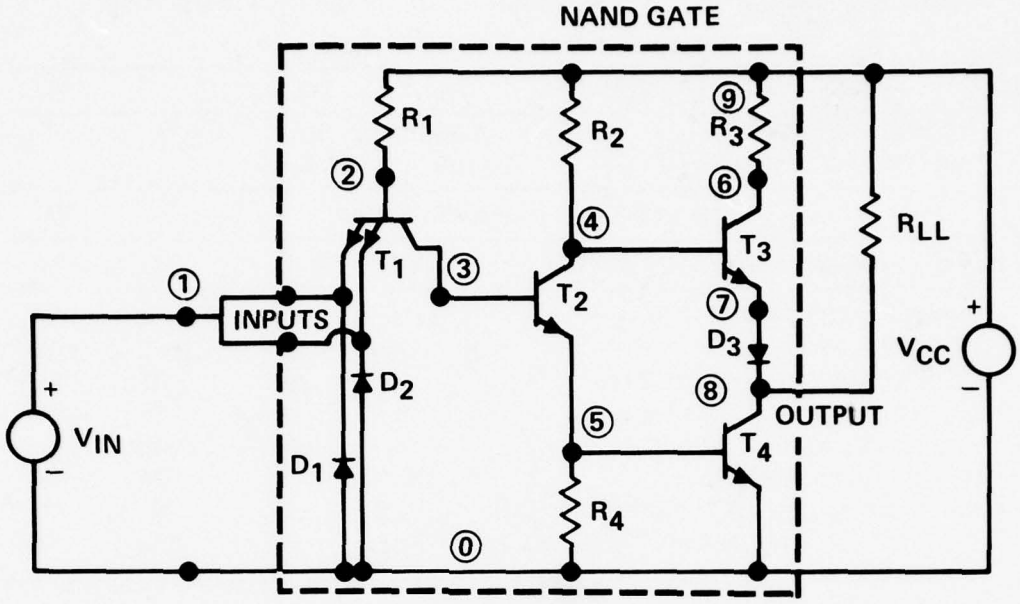


Figure 4.20. Schematic Diagram of 7400 NAND Gate with External Connections. Node Numbers for SPICE Simulations are Shown.

interference effects, while all other NAND gate components are modeled using the standard component models available in SPICE.

Parameters for the transistors and diodes in the 7400 NAND gate are listed in Table 4.2. These values were obtained from Reference [8] and were converted into a form usable by SPICE. These parameter values were entered as data in the SPICE simulations. Table 4.3 is an example of data for a SPICE simulation of an RF perturbed 7400 NAND gate.

Transistor T4, into which all the RF power was assumed injected, was modeled using the modified Ebers-Moll model shown in Figure 4.21. It was incorporated in the SPICE input data as an external model. (For a detailed description on using external models in the program SPICE, see Reference [5]). To implement the current-dependent current sources IAFIE and IARIC in the modified Ebers-Moll model, 1Ω current sensing resistors were placed in the emitter and collector as shown in Figure 4.21. The current source IAFIE ($\alpha_F I_F$) and IARIC ($\alpha_R I_R$) are made to depend upon the voltage drops $V_{12} - V_{13}$ and $V_{12} - V_{11}$ across resistors RESENSE and RCSENSE

Table 4.2. Diode and Transistor Parameter Values for the 7400 NAND Gate

DIODE PARAMETERS

NAME	PARAMETER DESCRIPTION	DIN	D3
RS	OHMIC RESISTANCE (Ω)	60	30
IS	SATURATION CURRENT (pA)	100	5

TRANSISTOR PARAMETERS

NAME	PARAMETER DESCRIPTION	T1	T2	T3	T4
BF	FORWARD BETA (βF)	.316	19.8	17.2	21.7
BR	REVERSE BETA (βR)	.0024	.060	.082	.106
RB	BASE OHMIC RESISTANCE (Ω)	68	75	70	80
IS	SATURATION CURRENT (pA)	.5	3	8	20
AF[a]	FORWARD ALPHA (αF)	.24	.952	.945	.956
AR[a]	REVERSE ALPHA (αR)	.0024	.057	.076	.0956
IES[a]	EMITTER DIODE SAT. CURRENT (pA)	2	3	8	20
ICS[a]	COLLECTOR DIODE SAT. CURRENT (pA)	200	50	100	200

[a]PARAMETER USED IN MODIFIED EBERS–MOLL MODEL.

Table 4.3 Data Cards for a SPICE Simulation of an RF Perturbed 7400 NAND Gate

```
VCC 9 0 DC 5
VIN 1 0 DC 4.25
VGEN 16 0
 *NODE 0 = NODE 20
R1  9 2 4.38K
R2  9 4 1.43K
R3  9 6 0.116K
R4  5 0 1.06K
RLL 8 9 9.11K
QT1 3 2 1 MOD1
QT2 4 3 5 MOD2
QT3 6 4 7 MOD3
XT4 8 5 0 16  RF-EBML
DIN 0 1 MOD5
D3  7 8 MOD6
 .MODEL MOD1 NPN .316  .0024  68
   IS=5E-13
 .MODEL MOD2 NPN 19.8  .060   75
   IS=3E-12
 .MODEL MOD3 NPN 17.2  .082   70
   IS=8E-12
 .MODEL MOD4 NPN 21.7  .106   80
   IS=2E-11
 .MODEL MOD5 D RS=60 IS=IE-10
 .MODEL MOD6 D   RS=30     IS=5E-12
 .DC TC VGEN   .2  20 .2
*BY CAUSING VGEN TO VARY THE
*CURRENT GENERATORS ISCC AND ISCE
 *WHICH DEPEND UPON THE VOLTAGE ACROSS
 *RSWEEP ALSO VARY, THIS SIMULATES
 *A CHANGE IN INCIDENT RF POWER.
 .OUTPUT VOUT 8 0   PLOT DC 0 5
 .TEMP 20
 *MDAC RF MODIFIED EBERS-MOLL MODEL
 .MODEL RF-EBML X 8 5 20  16
IAFIE V 8 12  12  13  0.956
IARIC V 20  12  12  11  0.0956
RBB  5 12  80
RCSENSE  12  11  1
RESENSE  12  13  1
DC1 11  8 MOD7
DE1 13  20  MOD8
 .MODEL MOD7  D IS=200P
 .MODEL MOD8  D IS=20P
 *RF  INDUCED TERMS (ELEMENTS)
RSWEEP 16  20  1
RGC  8 10  190
RGE  14  20  180
ISCC  V 10  8 16  20  3.79M
ISCE  V 14  20  16  20  0.667M
DC2 11  10  MOD7
DE2 13  14  MOD8
 .FINIS
 .END
```

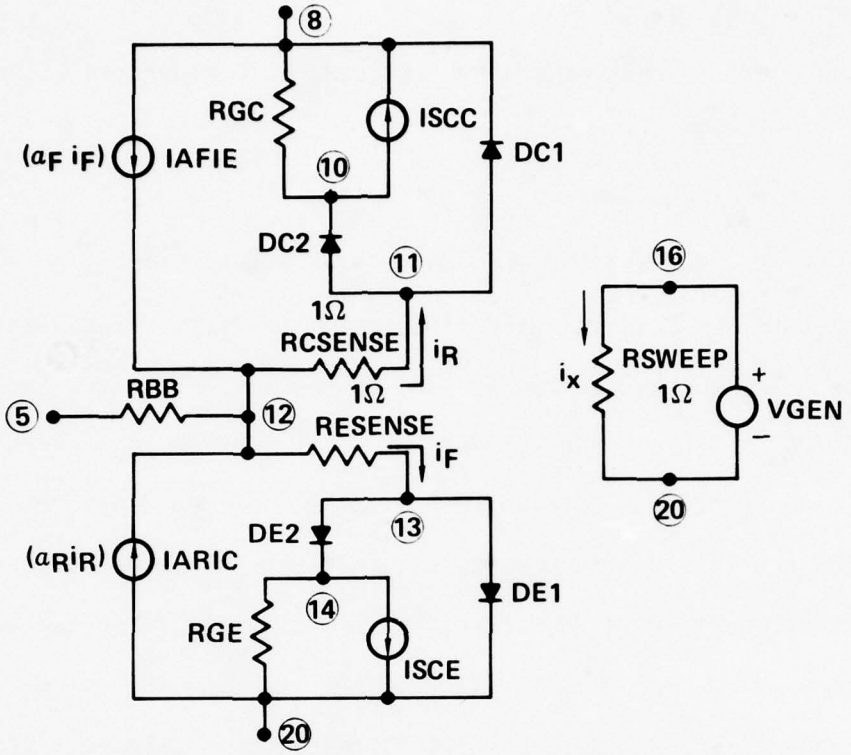


Figure 4.21. Modified Ebers-Moll Model in an External Model Configuration. Node Numbers for SPICE Simulations are Shown.

respectively. The result is that IAFIE = AF(V_{12} - V_{13}) and IARIC = AR(V_{12} - V_{11}) where the values for AF and AR (α_F AND α_R) are given in Table 4.2. Diodes DE1 and DE2 both have saturation current IES and diodes DC1 and DC2 both have saturation current ICS given in Table 4.2.

The dc voltage source VGEN shown in Figure 4.21 controls the voltage V_{16} - V_{20} which controls the RF induced dc current generators ISCE and ISCC. By causing VGEN to vary over an appropriate range, the values for ISCE and ISCC are made to vary also. This is how the RF power is swept in the computer simulations. The appropriate range of values for VGEN is determined from the relationship

$$PINC = VGEN^2/400\Omega, \tag{4.35}$$

where PINC is the RF power incident on the 7400 NAND gate. The value for PINC is assumed equal to the maximum available power from a Thevenin equivalent RF source of amplitude VGEN and impedance 50Ω. Equation (4.35) may be rewritten as

$$VGEN = (400\ PINC)^{0.5} . \quad (4.36)$$

The two RF induced dc current generators ISCE and ISCC depend on VGEN:

$$ISCE = (KE/RGE)VGEN \quad (4.37)$$

$$ISCC = (KC/RGC)VGEN. \quad (4.38)$$

The values of KE, KC, RGE and RGC were determined experimentally at 220 MHz for a 2N2369A transistor, which is believed similar to the output transistor T4 in the 7400 NAND gate. The values determined were KE = 0.12, KC = 0.72, RGE = 180Ω, RGC = 190Ω, KE/RGE = 0.67 m℧ and KC/RGC = 3.79 m℧. The ratios (KE/RGE) and (KC/RGC) are transconductances which relate the RF induced dependent current generators ISCE and ISCC to the control voltage VGEN. VGEN is related to the RF incident power by Equation (4.36). Varying VGEN over the range 0.2 to 20V corresponds to varying PINC over the range of 0.1 to 1000 mW. (A different procedure to relate ISCE and ISCC to PINC is described in the next section).

Three types of TTL NAND gates were investigated to determine their relative susceptibilities to RF interference. These are the normal 7400 series, the high speed 74H00 series, and the low power 74L00 series. The three NAND gate series use different values of internal resistances R1-R4 shown in Figure 4.20. The resistance values are given in Table 4.4. The variation in the values for R1

Table 4.4. Resistor Values for 7400 NAND Gate Type Variations

RESISTOR (kΩ)	7400	FAN-OUT	74H00	FAN-OUT	74L00	FAN-OUT
R1	4.38		2.80		40	
R2	1.43		0.70		20	
R3	0.116		0.116		0.116	
R4	1.06		1.06		12	
RLL	4.38	1	2.80	1	40	1
RLL	0.30	15	0.28	10	4	10

affects the value of the resistor RLL required to simulate different fanout values. The values of RLL required to give a low fanout (F = 1) and a high fanout (F = 10 or 15) are also given in Table 4.4.

Figure 4.22 shows a plot of the predicted values of the NAND gate output

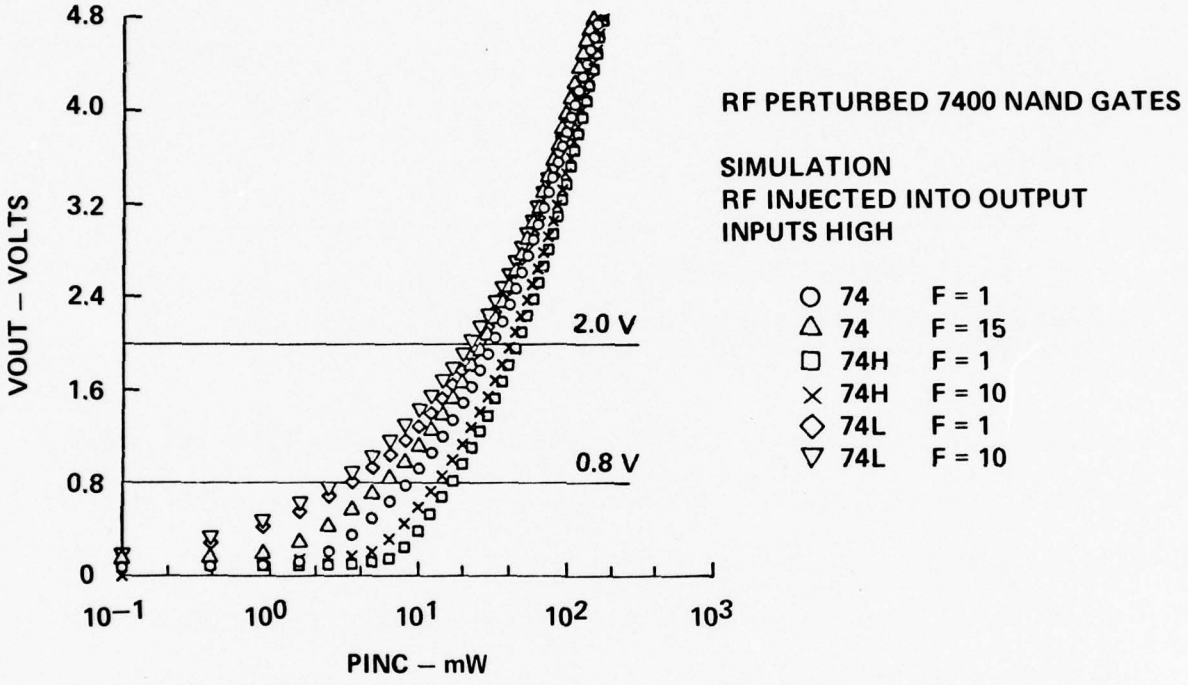


Figure 4.22. Output Voltage vs. Incident RF Power From SPICE Simulations of Three 7400 NAND Gate Types with Different Fanouts. Susceptibility Thresholds at V_{OUT} Equals 0.8 and 2.0 Volts are Shown.

voltage VOUT versus the incident RF power PINC. The plots show the relative susceptibilities of the three NAND gate types with low and high fanouts. When no RF power is applied, the output voltage is low (approximately 0.1V). As the RF power increases, the VOUT values increase until they cross the two susceptibility threshold levels. The threshold at VOUT = 0.8V corresponds to the highest voltage that a subsequent stage is guaranteed to recognize as a low state input. The value VOUT = 2.0V corresponds to a VOUT certain to be recognized as a high state (instead of a low state) by a subsequent TTL input. The values of RF power which cause these two threshold levels to be exceeded are given in Table 4.5.

Table 4.5. Values of RF Power Which Cause EM Susceptibility Criteria To Be Exceeded for Three 7400 NAND Gate Types

TYPE OF GATE	VOUT = 0.8V		VOUT = 2.0V	
	SPICE[a] P_I (mW)	EXP.[b] P_A (mW)	SPICE[a] P_I(mW)	EXP.[b] P_A (mW)
74L00 (F=10)	2.8		22	
74L00 (F=1)	3.5		25	
7400 (F=15)	5.8	4.0	28	28
7400 (F=1)	7.9		30	
74H00 (F=10)	13		40	
74H00 (F=1)	17		45	

[a]VALUES OF INCIDENT RF POWER.

[b]VALUES OF ABSORBED RF POWER. – SEE REF 4.10. VALUES OF INCIDENT RF POWER WOULD BE HIGHER.

The results shown in Table 4.5 indicate that the low power 74L00 series NAND gate is the most susceptible to RF interference, while the high speed 74H00 series is the least susceptible. For each NAND gate type the fanout value has a small effect (less than 2 dB difference between minimum and maximum fanout) upon the RF power required to cause the threshold levels to be exceeded. Also shown in Table 4.5 are experimental values for the absorbed RF power required to cause the 7400 series NAND gate output voltage to exceed the two susceptibility threshold levels[7]. The values predicted by the SPICE simulations are in good agreement with the experimentally measured values.

4.5 Worst Case Analysis of 7400 NAND Gates

In the previous section the variation in susceptibility of three types of TTL NAND gates was investigated. The interference effect was assumed to occur solely in the output transistor T4, which was assumed similar to a 2N2369A transistor in characteristics, and the modified Ebers-Moll transistor parameters used for T4 were values measured in the laboratory for the 2N2369A.

The possible values for the parameters of T4 may vary widely when the circuit

is located in an arbitrary electromagnetic environment where RF signals may be picked up by wires and cables. An induced RF signal can be represented by a Thevenin equivalent containing a voltage source and series impedance. In an actual situation, the equivalent impedance seen from the circuit will not be as well defined as in the laboratory, so we must take into account the effect of all possible source impedance values in a worst case simulation. This section describes a worst case analysis of a 7400 (standard series) NAND gate where the RF source impedance is not known a priori.

As in the previous section, RF is conducted into the output terminal of the 7400 NAND gate. Both inputs are assumed to have a high state voltage, and the output voltage is a low state in the absence of RF. As before, the RF is assumed to affect transistor T4 only. Earlier simulations[7] have shown that when RF power is injected into the collector of a transistor biased as T4 in the 7400 NAND gate the worst case results are obtained when all of the RF power is assumed to affect the collector-base junction, and none is assumed to reach the emitter-base junction. Thus, no rectification occurs in the emitter-base junction. The rectification in this junction is removed from the modified Ebers-Moll model by setting ISCE = 0 and RGE = ∞ (or a sufficiently large value) in Figure 4.21.

The collector-base junction rectification parameters of T4 were assigned using the information described in Section 4.3, where rectification parameter ranges were described for the case of completely arbitrary RF source impedance values. The collector-base junction was assumed lossless (certainly a worst case assumption) which means, from Equation (4.34) that RGC can assume any positive real value and that

$$K_C = (8/RGC)^{1/2} \tag{4.39}$$

where

$$ISCC = K_C(PINC)^{1/2}. \tag{4.40}$$

If we choose

$$PINC = VGEN^2/8\ RGC, \tag{4.41}$$

then from Equations (4.39) and (4.40),

$$ISCC = VGEN/RGC. \tag{4.42}$$

The program SPICE was used to perform a worst case analysis of the 7400 NAND gate. The value of external resistor RLL was set to 300Ω, corresponding to a fanout of 15. (Results of the previous section indicate that high fanouts lead to EM susceptibility at slightly lower RF power levels than low fanouts). The first step in the simulation procedure was to assign a value for the resistance RGC in the collector-base junction of T4. The range of 5 to 5000 ohms was simulated in the SPICE runs. (Even though RGC can assume any positive real value, the range $5 \leq RGC \leq 5000$ ohms is wide enough to include the values of RGC which give the worst case response. The results show this clearly. For other interference simulations a wider range of RGC may be necessary.)

The next step was to sweep the dc control voltage VGEN in the SPICE program over an appropriate range of voltages corresponding to the desired range of incident RF powers, as given by Equation (4.41). At each value of VGEN, the value of ISCC was given by Equation (4.42). As a final step, the values of the output voltage VOUT were plotted versus PINC. Then the process was repeated using a new value of RGC until adequate coverage of the entire range of RGC was obtained.

Figure 4.23 plots VOUT versus PINC from the SPICE simulation results. It can be seen that the value of RGC is quite influential in determining the shape of the VOUT versus PINC curve, and in determining the RF power levels at which various EM threshold levels are crossed. From Figure 4.23, the values of incident power required to cause VOUT to cross EM susceptibility threshold levels of 0.4, 0.8, and 2.0 volts were determined for each simulation. These values are plotted in Figure 4.24 versus the value of RGC for that case. Three curves result (one for

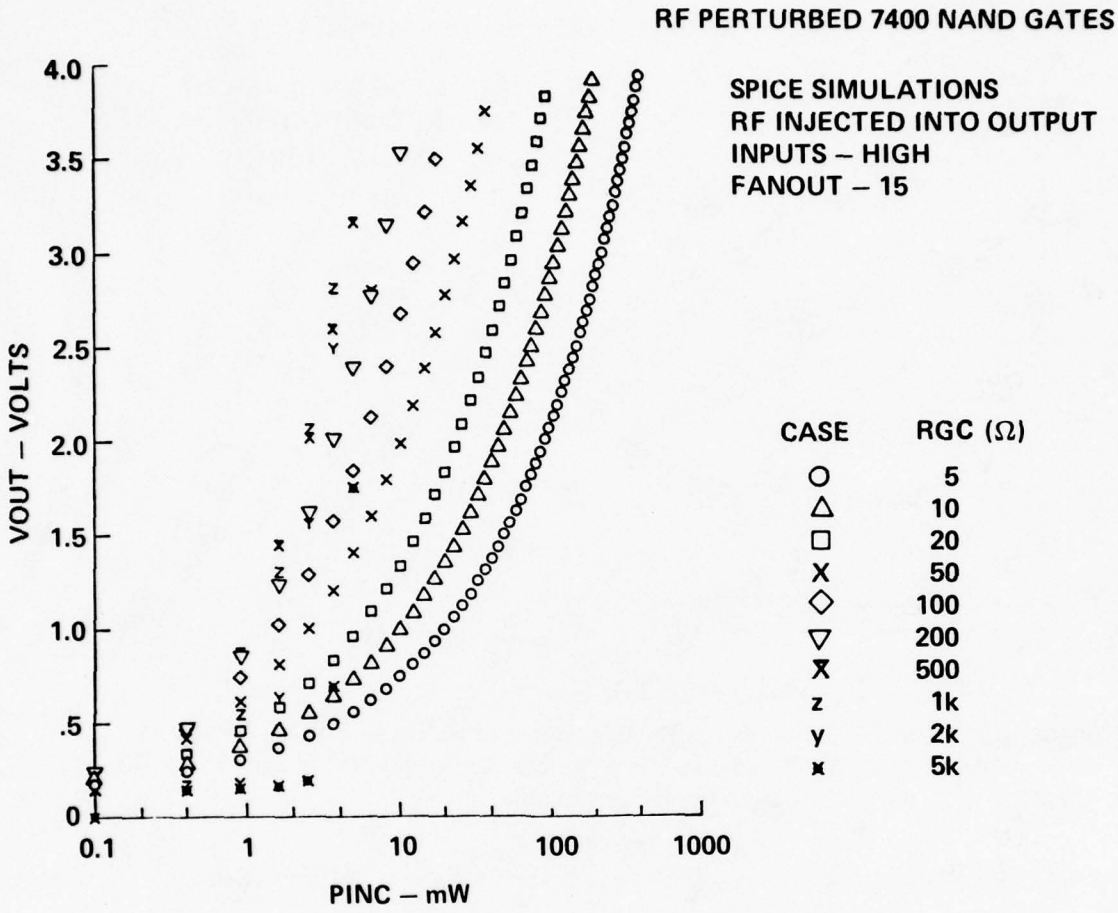


Figure 4.23. SPICE Simulation Values of Output Voltage versus Incident RF Power Level for a 7400 NAND Gate

each threshold level). It is observed from Figure 4.24 that for each susceptibility threshold level the PINC versus RGC plot has a minimum PINC value. The minimum values of PINC provide an estimate of the minimum incident RF power expected to cause the various EM susceptibility threshold levels to be exceeded.

Determining the values of these minima is the primary purpose of the worst case modeling. The range of RGC simulated should include the values at which these minima occur within the limits of RGC dictated by Equations (4.30) and (4.31). It can be seen that the range of RGC simulated here, 5 to 5000 ohms, is of sufficient width to include minima in each of the three curves in Figure 4.24. As an alternative, an iterative procedure can be used to locate these minima.

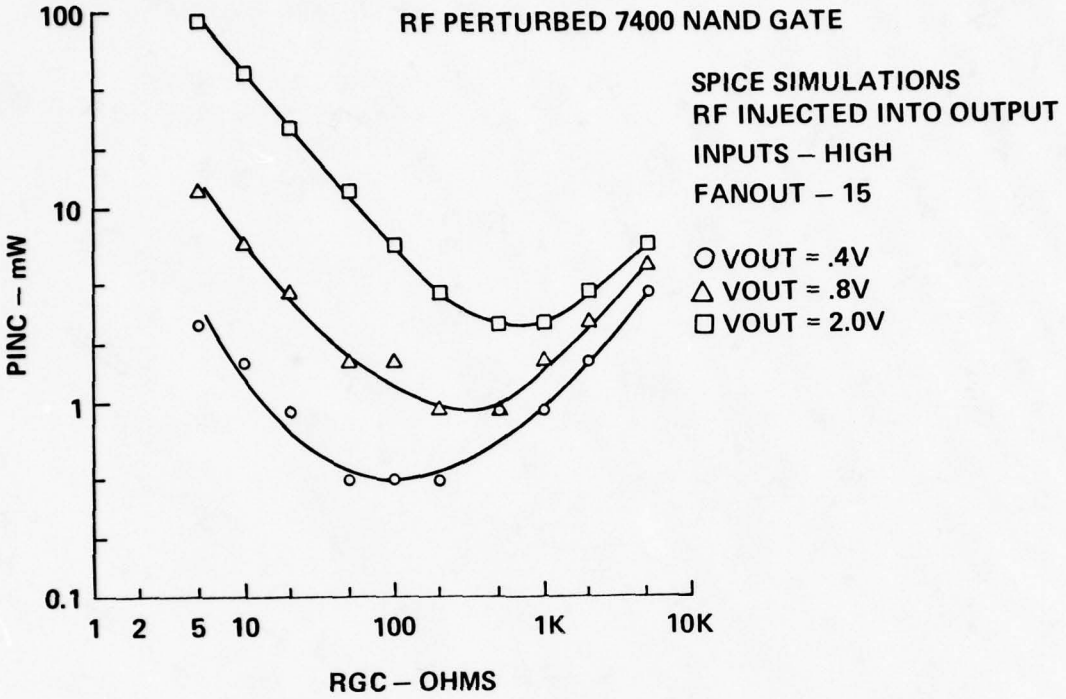


Figure 4.24. **Values of Incident RF Power Required to Cause Output Voltage of 7400 NAND Gate to Exceed Susceptibility Threshold Levels versus the RF Thevenin Source Impedance**

The minimum susceptibilities predicted in Figure 4.24 for thresholds of 0.4, 0.8, and 2.0 volts are plotted in Figure 4.25 on a graph of the measured worst case susceptibility curves for TTL devices. (A constant of proportionality was used to convert the predicted incident power values to absorbed power for Figure 4.25). Since the base-collector junction of T4 was assumed lossless, and the impedance of the Thevenin RF source was assumed completely arbitrary, in the worst case no frequency dependence enters the predicted susceptibility data.

The predicted worst case curves in Figure 4.25 lie below the measured worst case curves. This is reasonable, since the SPICE simulations analyzed a wider range of RF conditions than could reasonably be studied in the laboratory. Additionally, several conservative assumptions were made in the analysis: all of the interference effect is in the collector-base junction of T4, no loss exists in the collector-base junction, etc. The RF impedances used in the simulations

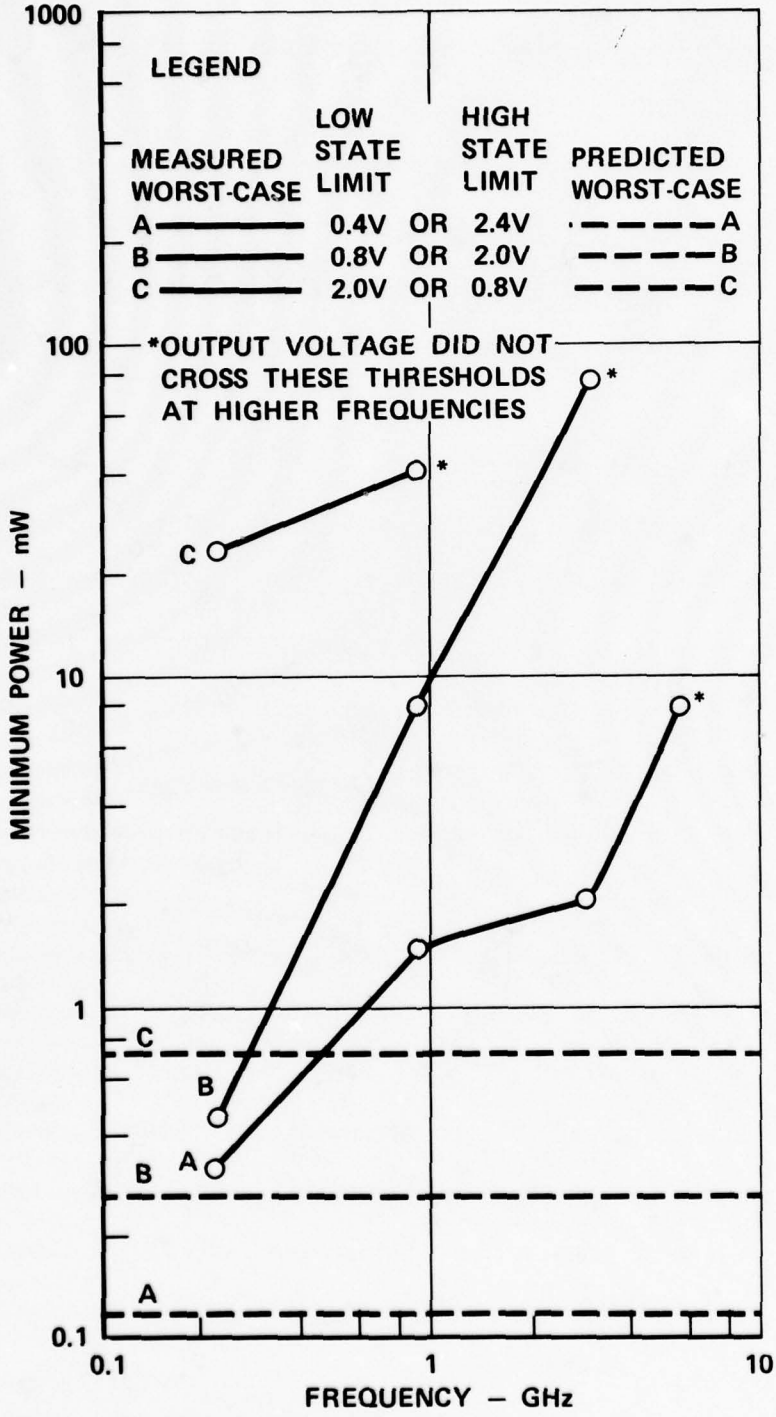


Figure 4.25. Worst Case Susceptibility Values for TTL Devices (Maximum Specification Value for Low V_{OUT} = 0.4 Volt and Minimum Specification Value for High V_{OUT} = 2.4 Volts)

included those typically encountered in actual interference environments. It is unlikely that RF powers below the predicted susceptibility levels will cause interference in any real-world application.

The worst case analysis procedure described in this section is quite general and can be applied to other electronic circuits or IC's. Comparison of the predicted worst case results for the 7400 NAND gate with the worst case results measured in the laboratory gives confidence that such a simulation procedure is valid.

4.6 Simulation of Interference in 741 Op Amps

Interference models for the 741 op amp were studied during this increment for the case of RF entering the input terminals. The study utilized macromodeling techniques, and a full-scale simulation of the complete circuit was done for comparison of the results. The modified Ebers-Moll transistor model was used to account for the interference effect, which was assumed to occur only in a single input transistor. This section describes the analysis of interference in a 741 op amp.

The op amp macromodel used was previously published by Boyle, et. al[9], and is illustrated in Figure 4.26. Much of the internal structure of the op amp has been replaced with functional equivalents. This reduces the amount of computer time required to obtain a solution, because the macromodel has fewer elements than the operational amplifier, and because much of the circuit consists of linear elements, instead of nonlinear elements such as transistors and diodes. At its terminals, however, the op amp macromodel behaves like an actual op amp. Table 4.6 lists the macromodel parameters.

A significant feature of the macromodel created by Boyle is that it retains the differential pair configuration at the input terminals, as is found in an actual 741. The two transistors at the input of the macromodel perform the same

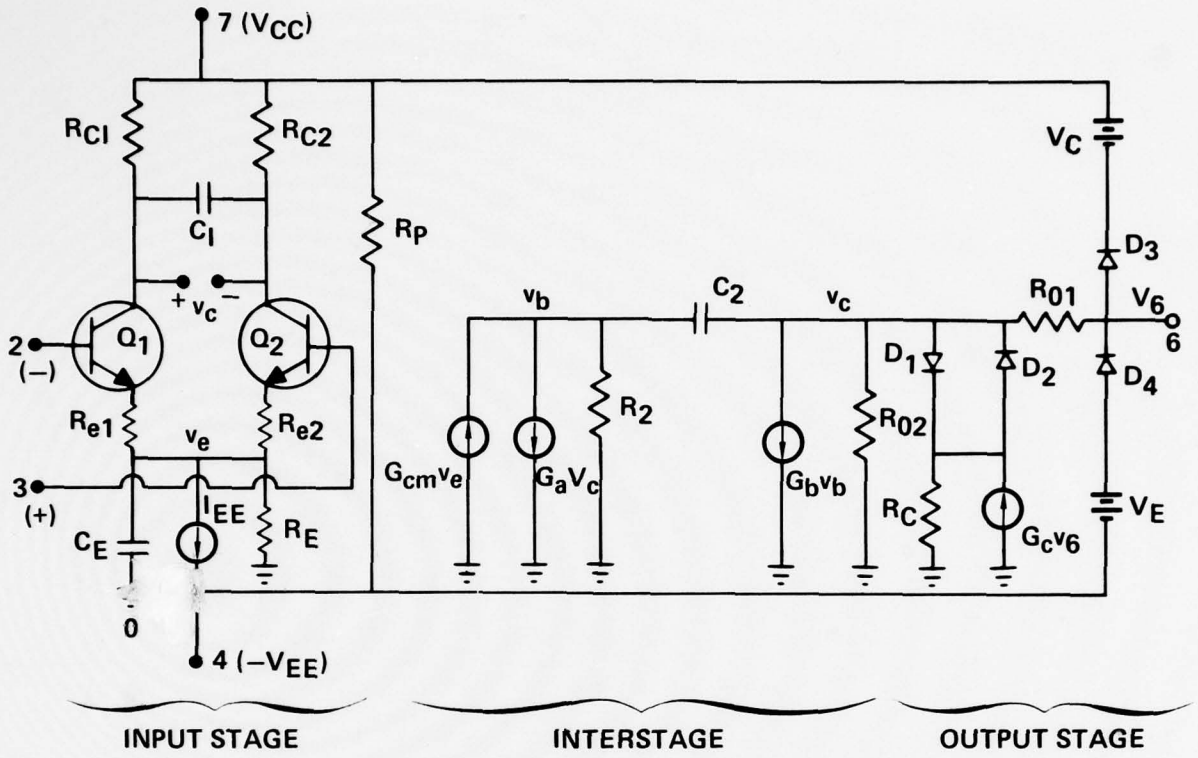


Figure 4.26. 741 Op Amp Macromodel

functions as their counterparts in the actual device. The macromodel uses an Ebers-Moll transistor model for each input transistor.

With RF entering the input of the op amp, it was postulated that the interference effect could be accounted for by replacing the transistor model at that input with a modified Ebers-Moll transistor model, which includes RF effects. Figure 4.21 shows the modified Ebers-Moll transistor model used in the simulations. The input transistors were assumed similar to 2N930A transistors in characteristics. RF parameters were inferred from measured 2N930A data. Table 4.7 lists the modified Ebers-Moll parameters at 220 MHz. In the macromodel simulations, only the transistor at the RF input was modeled with a modified Ebers-Moll model; the other input transistor used a standard Ebers-Moll model having the same parameters (except RF parameters) as the modified model.

When RF enters the base of a transistor it has been observed that the

Table 4.6. Macromodel Parameters for LM 741

T	300°K
I_{SD3}	8×10^{-16}A
R_2	100 kΩ
C_2	30 pF
C_E	2.41 pF
β_1	150 (NO RF)
β_2	150 (NO RF)
I_{EE}	20.26 μA
R_E	9.872 MΩ
R_{C1}	5305 Ω
R_{e1}	2712 Ω
C_1	5.460 pF
G_a	188.6 μmho
G_{CM}	6.28 nmho
R_{01}	32.13 Ω
R_{02}	42.87 Ω
G_b	247.49 mho
I_{SD1}	8×10^{-16}A
R_C	0.02129×10^{-3} Ω
G_C	49964 mho
V_c	1.803 V
V_E	2.303 V

transistor beta appears to decrease[10]. This effect was included in the modified Ebers-Moll models for the input transistors. Figure 4.27 is a plot of the forward beta vs. RF power, obtained from 2N930A data, that was used in the simulations.

The op amp was simulated in a feedback amplifier circuit with a gain of -10 as shown in Figure 4.28. This corresponds to the circuit used when op amp susceptibilities were tested in the lab. The input voltage is 0.5 volts, so the expected output voltage with no RF is -5.0 volts.

The circuit was simulated on ISPICE, a timesharing version of the program SPICE which is available through National CSS, Inc. Figure 4.29 is a listing of

Table 4.7. Modified Ebers-Moll Parameters for Op Amp Input Transistors

α_F = 0.993377 (NO RF)

α_R = 0.6666

$I_{DE1} = 5.067 \times 10^{-14} \left(e^{\frac{q}{kT} V_{DE1}} - 1\right)$ AMPS

$I_{DE2} = 3.4 \times 10^{-14} \left(e^{\frac{q}{kT} V_{DE2}} - 1\right)$ AMPS

RGC = 1KΩ

RGE = 100Ω

$ISCC = 0.01\sqrt{P_{RF}}$ AMPS

$ISCE = 0.17\sqrt{P_{RF}}$ AMPS

WHERE P_{RF} IS RF POWER IN WATTS.

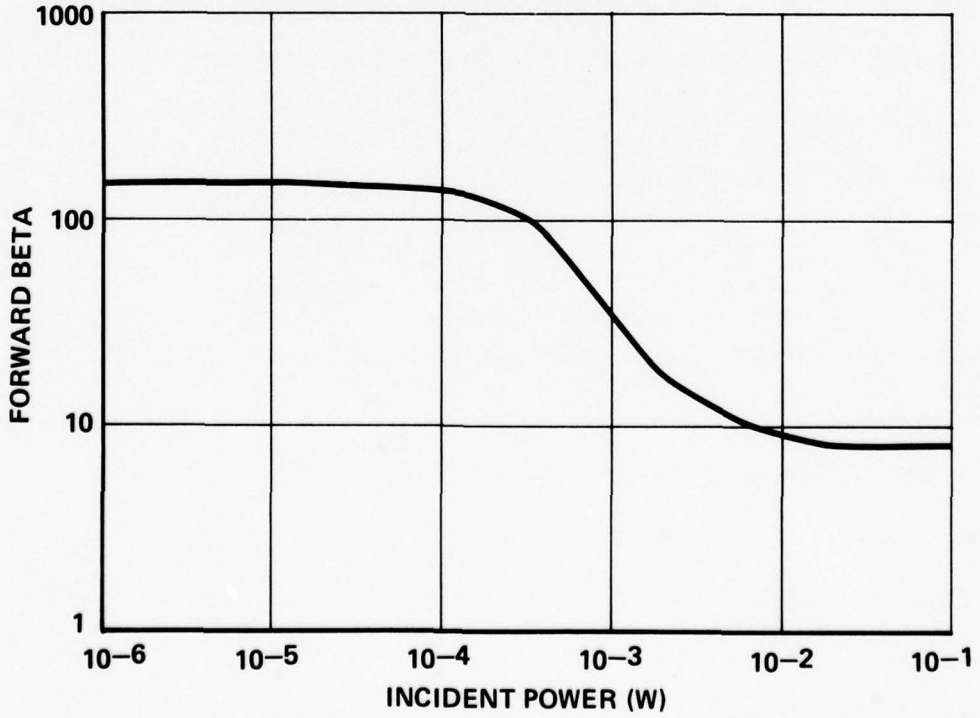


Figure 4.27. Forward Beta vs. Incident RF Power Used in Modified Ebers-Moll Model for Op Amp Input Transistors

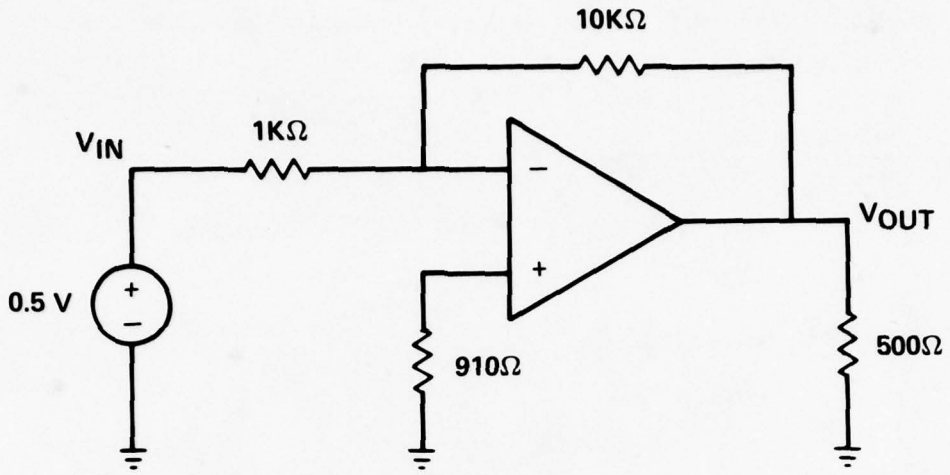


Figure 4.28. Closed Loop Amplifier Circuit Used in Op Amp Simulations

the input statements for an RF simulation. The input command structure is similar to that used in SPICE, but several additional features are available. One example is that circuit element values may be made functions of an independent variable. In the listing of Figure 4.29, RFPWR is an independent variable specifying the RF power level. The values of current sources ISCC and ISCE are then made functions of the RF power level with the commands

```
ISCC        4        1        XC(RFPWR)
ISCE        7        3        XE(RFPWR)
```

where XC(RFPWR) and XE(RFPWR) are functions of the RF power level specified by the *following statements:*

```
XC(RFPWR) = 0.01 * (RFPWR) ** .5
XE(RFPWR) = 0.17 * (RFPWR) ** .5.
```

Another feature available in ISPICE is that element values may be specified in tabular form versus an independent variable. In Figure 4.29, the forward alpha is tabulated versus RF power in the statement

```
FAFIE    1    2    2    6    TABLE(RFPWR 0, .9933, .125M, etc.)
```

```
FILE: AMP-741  CKT      FROM: F DISK

RL 15 0 500
RFD 15 1 10K
RIN+ 0 2 910
RIN- 16 1 1K
RC1 7 5 5305
RC2 7 6 5305
RE1 3 9 2712
RE2 4 9 2712
RE  9 0 9.872MEG
R2 10 0 100K
RO1 11 15 32.13
RO2 11  0 42.87
RC  12  0 0.02129M
C1   5  6 5.46P
C2  10 11 30P
CE   9  0 2.41P
D1  11 12 DILIM OFF
D2  12 11 DILIM OFF
D3  15 13 DVLIM OFF
D4  14 15 DVLIM OFF
* 'OFF' INDICATES THAT THE ASSOCIATED DIODE IS OFF FOR
*  INITIAL ANALYSIS
XQ1  5  1  3 EB-MOL1
XQ2  6  2  4 RF-EBMOL(RFPWR)
* 'RFPWR' IS THE VARIABLE REPRESENTING THE RF POWER
* 'RFPWR' WILL BE SWEPT OVER A USER DETERMINED RANGE
* 'X' AS THE FIRST LETTER OF AN ELEMENT NAME INDICATES
* A CALL TO A SUBCKT
VIN1 16 0 VIN1
VC   7 13 DC 1.803
VE  14  8 DC 2.303
VCC  7  0 DC 12
VEE  8  0 DC -12
IEE  9  8 DC 20.26U
GCMVE  0 10  9  0 6.28N
GAVA  10  0  5  6 188.6U
GBVB  11  0 10  0 247.49
GCV15  0 12 15  0 46.964K
* ELEMENTS BEGINNING WITH 'G' ARE VOLTAGE CONTROLLED CURRENT SOURCES
MODEL DILIM D(IS=8E-16)
MODEL DVLIM D(IS=8E-16)
ISPICE: >
```

Figure 4.29. List of Input Statements for ISPICE Simulation of 741 Macromodel Including RF Effects

When executing, the values of the independent variables must be specified, and if desired, they may be stepped over a range of values. The latter procedure was used to obtain values of output voltage vs. the RF power level. Additional information on ISPICE features and command structure can be found in the ISPICE Reference Manual[11].

Curve (a) in Figure 4.30 shows the output voltage of the circuit vs. RF power level when RF enters the inverting input, and compares it to data measured in the laboratory[12], shown as X's. The output voltage decreases as the input

```
FILE: RF-EBMOL SUBCKT   FROM: F
RF-EBMOL(RFPWR)
* 'RFPWR' IS THE VARIABLE REPRESENTING THE RF POWER
* 'RFPWR' WILL BE SWEPT
NODES(1 2 3)
* (1 2 3 ) MUST CORRESPOND TO THE NODES ON THE SUBCKT CALL IN CKT
RCSENSE 5 2 1
RESENSE 6 2 1
RGC 4 1 1K
RGE 7 3 100
GAFIE  1 2 2 6 TABLE(RFPWR,0,.9933,.125M,.9926,.35M,.9906,1.85M,.9474,&
                    4.4M,.9130,19M,.8989)
* ELEMENTS IN THE LIST TABLE ARE OF   E FORM:
* (RFPWR,ALPHA,RFPWR,ALPHA,RFPWR,ALPHA.....)
GARIC  3 2 2 5 0.666
* ELEMENTS BEGINNING WITH 'G' ARE VOLT. CONTROLLED CURRENT SOURCES
ISCC    4 1 XC(RFPWR)
ISCE    7 3 XE(RFPWR)
* 'XC()' AND 'XE()' ARE CALLS TO FUNCTION FILES
* THE FUNCTION FILES DETERMINE THE  AMOUNT OF
* RF POWER INTO THE COLLECTOR AND THE AMOUNT INTO THE EMITTER
DC1     5 1 DC OFF
DC2     5 4 DC OFF
DE1     6 3 DE
DE2     6 7 DE OFF
* 'OFF' INDICATES THAT THE ASSOCIATED DIODE IS OFF FOR
* INITIAL ANALYSIS
MODEL DC D(IS=5.067E-14)
MODEL DE D(IS=3.4E-14)
ISPICE: >
```

```
FILE: EB-MOL1  SUBCKT   FROM: F DISK

EB-MOL1
* STANDARD EBERS MOLL MODEL
NODES(1 2 3)
* (1 2 3) MUST MATCH THE NODES ON THE SUBCKT CALL CARD IN CKT
RBB 2 6 1
RCSENSE 4 6 1
RESENSE 6 5 1
GAFIE   1 6 6 5 .9933
GARIC   3 6 6 4 0.6667
* 'G' INDICATES A VOLTAGE CONTROLLED CURRENT SOURCE
DE1     5 3 DE
DC1     4 1 DC OFF
MODEL DE D(IS=3.4E-14)
MODEL DC D(IS=5.067E-14)
ISPICE: >
```

Figure 4.29. (Continued) List of Input Statements for ISPICE Simulation of 741 Macromodel Including RF Effects

power increases until the amplifier reaches saturation. The simulation data is conservative compared to the measured data by approximately 4 dB. This is reasonable, however, because it was assumed that the incident power affects only the input transistor. In reality, it is unlikely that all of the incident RF power actually reaches the input transistor. Some is probably absorbed in other parts of the chip, or bypasses the input transistor through shunt capacitance. Curve (a) in Figure 4.31 shows the output voltage vs. RF power when RF enters the noninverting input and compares it to the measured case (X's). Again, the calculations are conservative by about 4 dB.

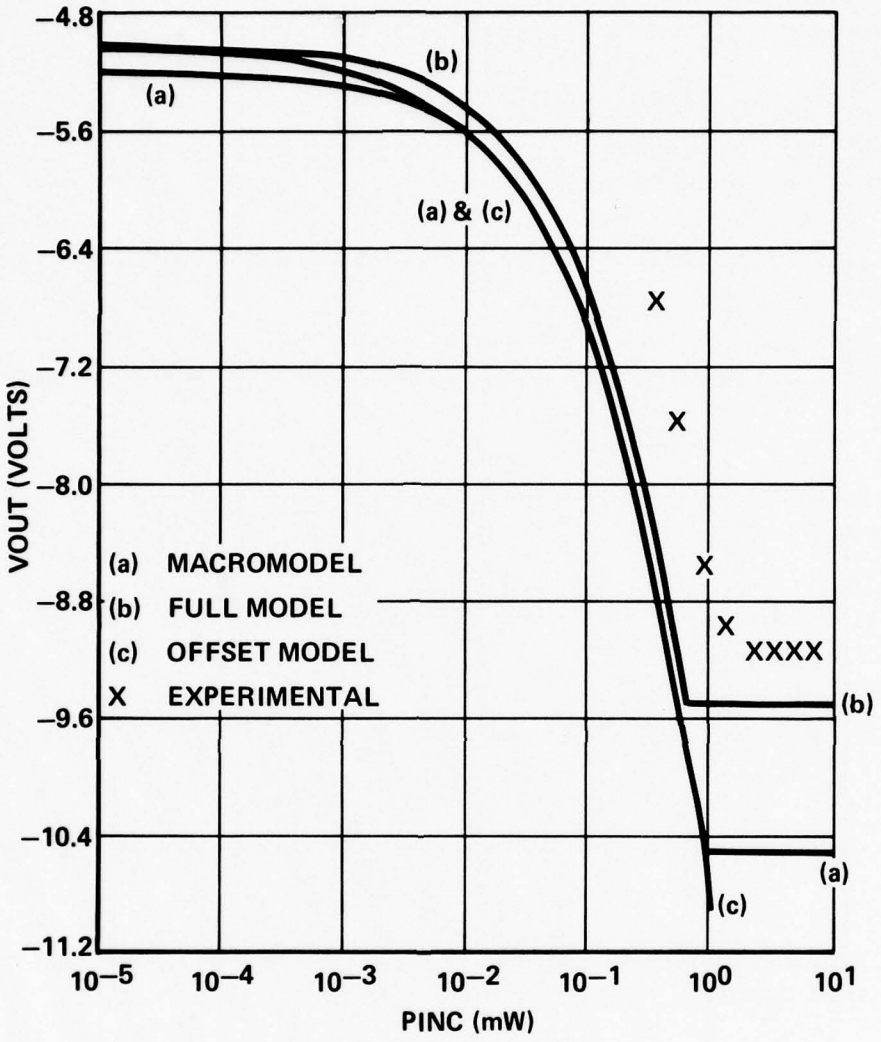


Figure 4.30. Output Voltage of Amplifier Circuit vs Incident RF Power. RF Conducted into Inverting Input of 741 at 220 MHz.

The voltages at which the macromodel saturates are different than the saturation voltages actually observed. The macromodel saturates at -10.5 volts and at +11.0 volts, where the supply voltages used were ±12 volts. The actual op amp saturates at -9.2 and +10.1 volts. These differences indicate that the values of V_E and V_C, which control the saturation voltages in the macromodel, should be adjusted if better agreement is desired. The saturation voltages are independent of the interference effects.

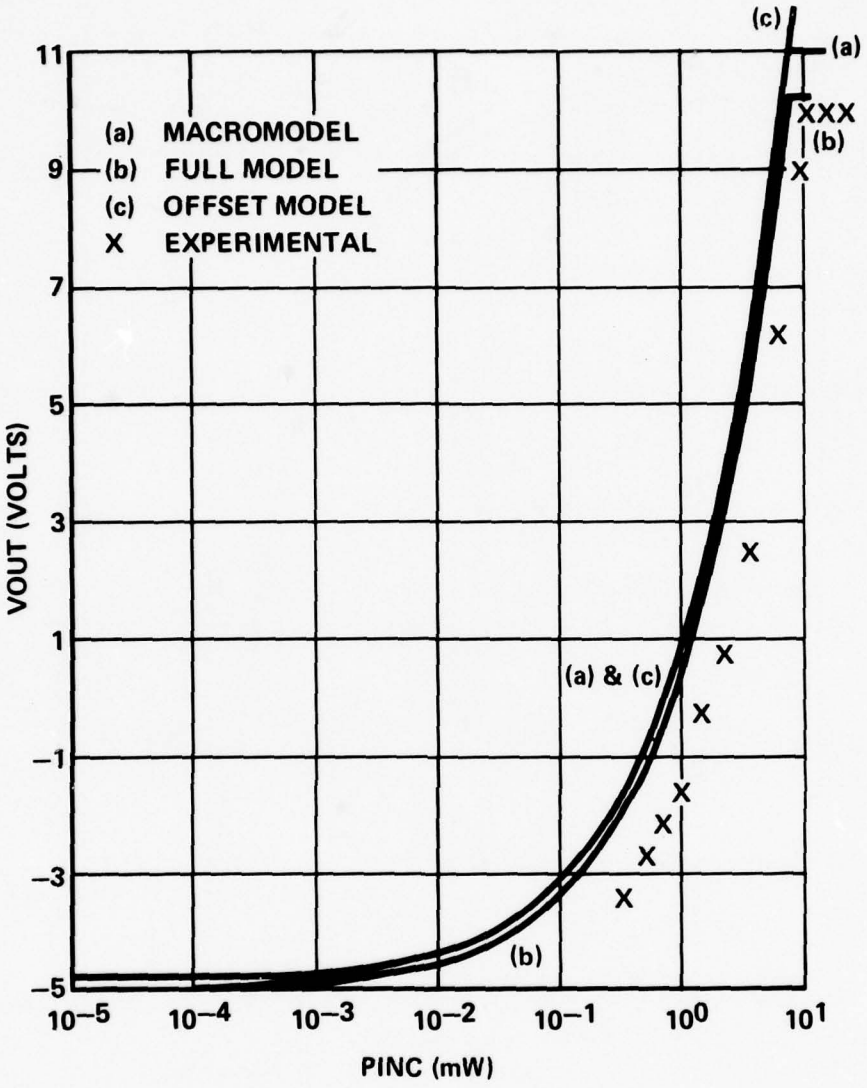


Figure 4.31. Output Voltage of Amplifier Circuit vs Incident RF Power. RF Conducted into Noninverting Input of 741 at 220 MHz.

A complete model of the 741 op amp has also been simulated for comparison with the macromodel simulation results. The complete model simulations used the computer program SPICE 2, an updated version of SPICE. A schematic diagram for the 741 op amp is shown in Figure 4.32. Both of the differential pair input transistors were modeled using the modified Ebers-Moll transistor model shown in Figure 4.21. (This procedure differs from that used with the macromodel, where

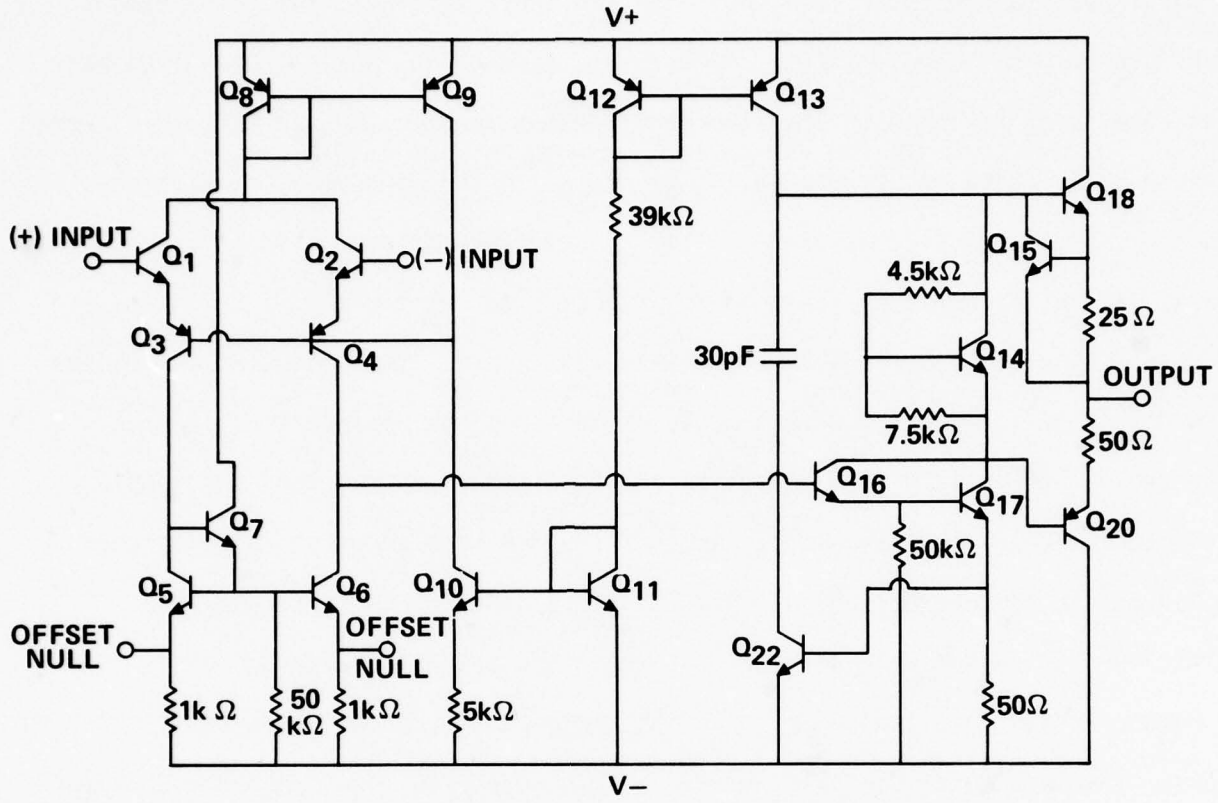


Figure 4.32. Schematic Diagram of 741 Op Amp Used in Complete Circuit Simulations

only the input transistor at the RF input terminal was modeled with a modified Ebers-Moll transistor model and the other input transistor was modeled with a standard Ebers-Moll model). Standard SPICE 2 components were used for all other op amp components, including transistors Q3-Q22. The parameters for Q3-Q22 are listed in Table 4.8.

Table 4.8. Parameter Values for the Transistors in the Complete Op Amp Model

NAME	PARAMETER DESCRIPTION	NPN's	PNP's
BF	FORWARD BETA	100	100
BR	REVERSE BETA	5	5
RB	BASE RESISTANCE (Ω)	5	5
RC	COLLECTOR RESISTANCE (Ω)	50	50
RE	EMITTER RESISTANCE (Ω)	1	1
IS	SATURATION CURRENT (pA)	0.01	0.01

To simulate RF injected into the inverting input terminal, the RF-dependent current generators ISCE and ISCC of Q2 were assigned values while those of Q1 were set to zero. For RF injected into the noninverting input, ISCE and ISCC of Q1 were activated while those of Q2 were set to zero. As in the macromodel simulations, transistors Q1 and Q2 were assumed similar to 2N930A transistors in characteristics. Table 4.7 lists the modified Ebers-Moll parameters for Q1 and Q2.

Curve (b) of Figures 4.30 and 4.31 show the complete model simulation results obtained when RF is injected into the inverting input and noninverting input, respectively. Comparison with Curve (a) in these figures shows that the complete op amp model and the macromodel give essentially the same results. A difference is noted in the voltages at which the output saturates. The complete model predicts the saturation voltages much more accurately than the macromodel.

Another difference is seen between the macromodel and complete model simulation results. The macromodel exhibits an offset voltage at its input when the RF power level is zero, which can be seen at low power levels (10^{-5} mW) as a 0.19 volt offset from the actual no-RF output voltage value of -5.00 volts. This offset occurs because of the different procedures used to represent the interference effect in the differential pair input circuit. In the macromodel, only the input transistor stimulated by the RF was modeled with a modified Ebers-Moll transistor model. This contains additional elements not found in the standard Ebers-Moll model (which is used for the other input transistor) which unbalances the differential pair circuit even when the RF power level is zero. Modeling both input transistors with the modified Ebers-Moll model, as in the complete model simulations, preserves the balance of the differential pair and prevents an extraneous offset voltage at the input. In subsequent macromodel simulations, it is recommended that both input transistors be modeled with modified Ebers-Moll models to prevent input offset voltages at zero RF power level.

Earlier observations had noted that the output offset voltage is directly proportional to the offset voltage at the input terminals of the op amp. This led to a simplified model of interference in op amps where the interference effect is represented as an input offset voltage generator, v_{II}, in series with the op amp input terminals. The relationship between v_{II} and the RF power level would be known, or could be determined mathematically or experimentally. A similar effect is observed in the computer simulations.

In Figure 4.33 an inverting amplifier circuit is shown which is the same as

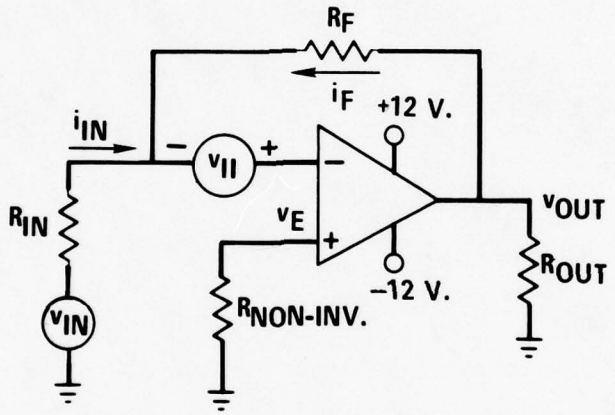


Figure 4.33. Inverting Amplifier Circuit with Offset Generator Shown at Op Amp Inverting Input Terminal

that used in the macromodel and complete model simulations and which includes the offset generator v_{II} at the op amp inverting input terminal. The output voltage can be shown to be

$$v_{OUT} = -v_{IN} \frac{R_F}{R_{IN}} - v_{II} \left(\frac{R_F}{R_{IN}} + 1\right). \tag{4.43}$$

In the circuit shown in Figure 4.28, $R_{IN} = 1K\Omega$, $R_F = 10K\Omega$, and $v_{IN} = 0.5V$, so

$$v_{OUT} = -5 - 11v_{II} \text{ volts.} \tag{4.44}$$

Good correlation has been found between the computer-calculated output voltages, and the output voltage predicted by Equation (4.44) where the input offset voltage was the product of ISCE and RGE (Figure 4.21). Thus,

$$V_{II} = ISCE \star RGE$$
$$= 17\sqrt{P_{RF}} \text{ volts} \qquad (4.45)$$

where P_{RF} is the RF power level in watts. A plot of the output voltage using (4.44) and (4.45) is compared in Figures 4.30 and 4.31 with the output voltage from the computer simulations. The correlation is found to be excellent. Therefore, the input offset voltage is seen to be the open circuit voltage of the Norton equivalent in the base-emitter junction of the input transistor, which arises from rectification of the RF signal in this junction.

This result can be seen in another way. In the op amp, the input transistors are in a differential pair circuit. Figure 4.34 shows a basic differential pair circuit where both transistors have been replaced by modified Ebers-Moll models. In the op amp, both of the input transistors are biased in an "on" state by the current source I_E which drives the differential pair. As such, many of the elements in the transistor models are inactive. Figure 4.35(a) shows the differential pair after removal of the inactive elements. The collector junctions have been removed, since they are reverse biased and do not conduct, and the current-controlled current sources $\alpha_R I_{R1}$ and $\alpha_R I_{R2}$ have also been removed.

In Figure 4.35, RF is assumed to enter the leftmost transistor, and the RF power level is assumed large enough so that most of the current I_{F1} flows through diode D_{XE1}, so diode D_{E1} was removed. In addition, the Norton equivalent I_{XE1} and R_{XE1} has been replaced with its Thevenin equivalent V_{XE1} and R_{XE1}, where

$$V_{XE1} = I_{XE1} R_{XE1}. \qquad (4.46)$$

In the rightmost transistor, I_{XE2} is zero (because no RF power enters this transistor), so most of the current I_{F2} flows through diode D_{E2}. Therefore elements D_{XE2}, I_{XE2} and R_{XE2} were also removed in Figure 4.35(a).

It is apparent in Figure 4.35(a) that, because the current source $\alpha_F I_{F1}$ in the left-hand branch of the differential pair can have any voltage across it, the

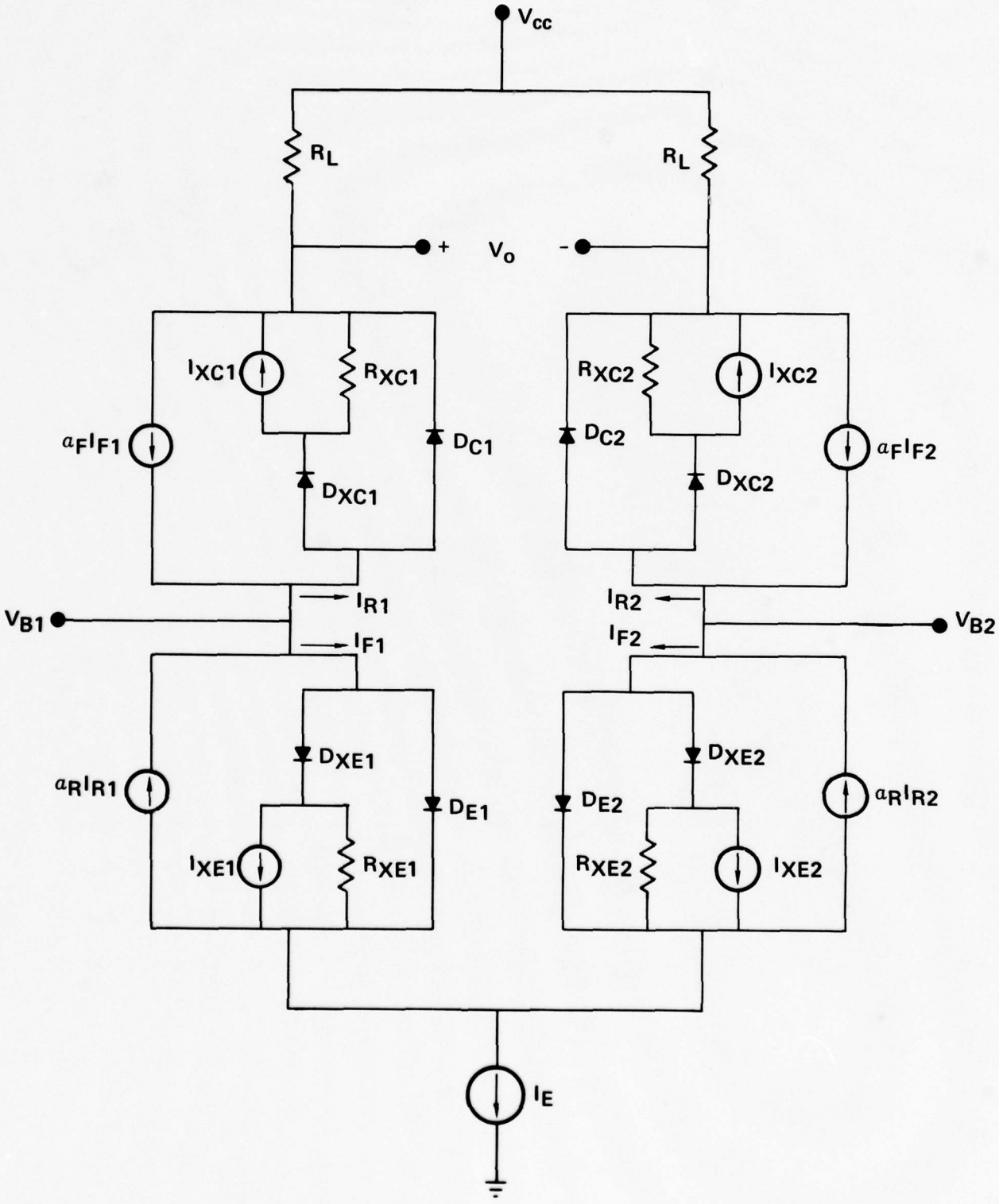


Figure 4.34. Basic Differential Pair Circuit With Transistors Replaced with Modified Ebers-Moll Models.

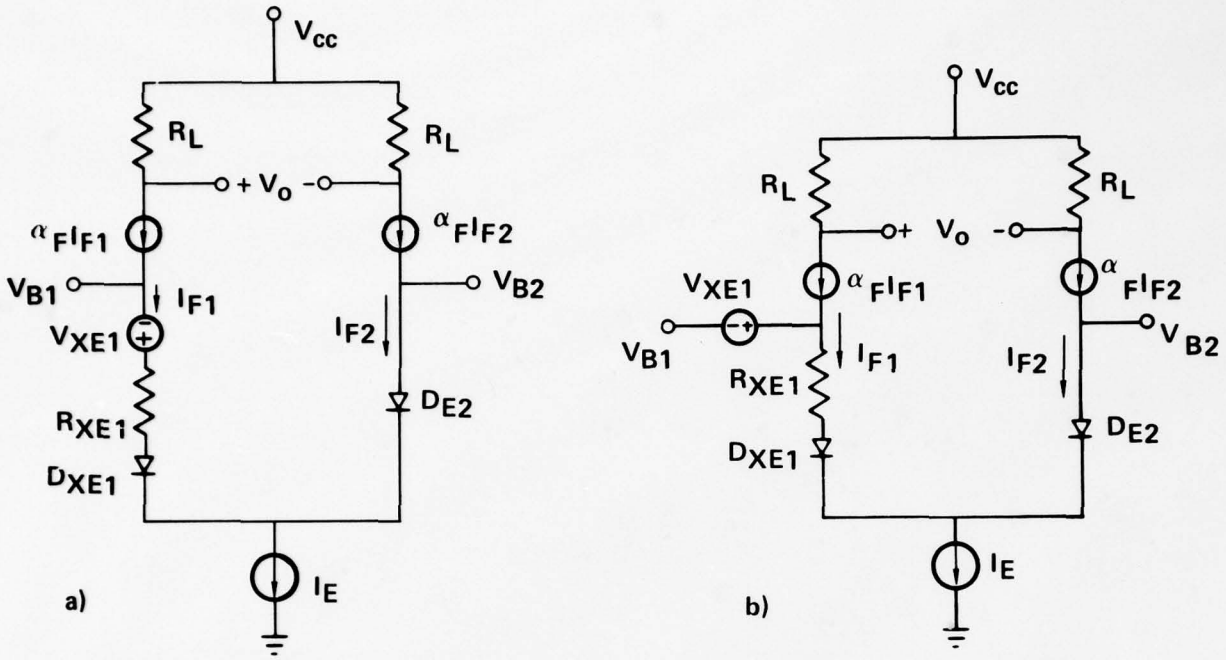


Figure 4.35. Simplification of Basic Differential Pair Circuit . RF Enters Leftmost Transistor .

voltage source V_{XE1} can be moved into the base lead of the left transistor, as shown in Figure 4.35(b). The offset voltage corresponding to v_{II} in Figure 4.33 is then

$$v_{II} = V_{XE1} - I_{F1} R_{XE1}. \tag{4.47}$$

The value of $I_{F1} R_{XE1}$ is insignificant compared to V_{XE1} (remember the RF power level was assumed large enough that most of I_{F1} flows through D_{XE1}, which implies that V_{XE1} would be significantly larger than $I_{F1} R_{XE1}$). Therefore, the voltage drop across R_{XE1} can be neglected. The simplified model shown in Figure 4.33 then follows where

$$v_{II} \approx I_{XE1} R_{XE1}. \tag{4.48}$$

The various modeling procedures described in this section have led to a greater insight of the interference effects in op amps. Additionally, a simplified offset model has been shown to be related to the more elaborate modeling procedures via the modified Ebers-Moll transistor model. The offset model has the

advantages that it is simpler to use than either of the computer simulation models, and can be used for quick "pencil and paper" types of calculations. The macromodel approach may be more accurate in some situations, and also could be used to find circuit responses when modulated signals are present because the op amp is modeled in greater detail, including its transient response properties. The complete op amp simulation approach is the most difficult, and requires more computer time than the macromodel approach, but has the advantage that interference effects at other terminals besides the inputs can be simulated by replacing the appropriate transistors and diodes by their interference models.

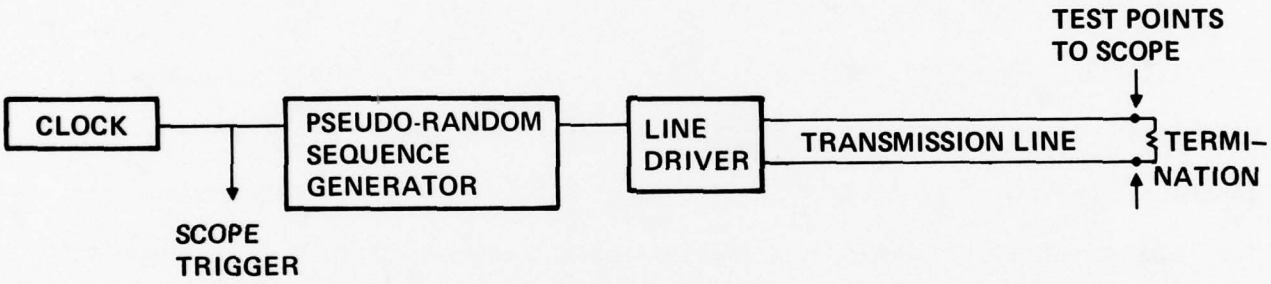
4.7 Signal Quality in Data Transmission Systems

Investigations into the RF susceptibility of line drivers and receivers have established that the receiver input threshold may change when stimulated by RF. The receiver input threshold is that voltage, applied differentially between the two receiver inputs, at which the receiver output changes state. As an example, Figure 3.6 shows the input-output transfer characteristics for a 9615 line receiver. At input voltages less than -0.08 volts, the output voltage is 5.0 volts (a high state). For input voltages greater than -0.08 volts, the output voltage is 0.2 volts (a low state). The input voltage -0.08 volts is referred to as the input threshold.

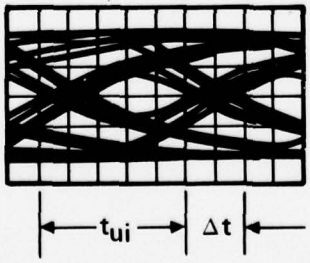
Threshold offsets, such as those caused by RF, have two undesirable effects on the signal quality in a data transmission system. First, a threshold offset will decrease the noise margin of the system, increasing the probability that spurious bits will enter the data stream in a noisy environment. The second effect, and the one which is addressed in this section, is that the signal may experience time variations in the received signal from those sent by the driver. A comparison of the transmitted and received waveforms may show that some pulses have become shifted in their relative position in the train, and some pulses may appear longer or shorter than in the original signal. Reference [13] discusses these time

variations quantitatively in a term called "percent jitter". This is a ratio of the maximum variation in pulse position or width to the minimum pulse period.

In order to get a laboratory measure of the percent jitter in a data transmission system, Reference [13] introduces an oscilloscope pattern called a "binary eye pattern" which is obtained when a random NRZ (nonreturn to zero) signal of minimum pulse width t_{ui} (a "unit interval") is transmitted down the line and the actual transmission line voltage at the receiver is observed with the oscilloscope. The pattern displayed on the scope is the binary eye pattern. Figure 4.36(a)



A) TEST SETUP TO PRODUCE BINARY EYE PATTERN



$$\text{PERCENT JITTER} = \frac{\Delta t}{t_{ui}} \times 100\%$$

B) BINARY EYE PATTERN

Figure 4.36. Jitter Measurement With Binary Eye Patterns

is a diagram showing how the display is obtained, and Figure 4.36(b) illustrates a typical binary eye pattern. The pattern consists of the superposition of the voltage waveforms seen at the termination due to the pseudo-random sequence generator. Because of the capacitance of the line, the voltage at the termination cannot change instantaneously, and exhibits the charging behavior evident in Figure 4.36(b). Referring to Figure 4.36(b), Fairchild defines percent jitter as

$$\text{percent jitter} = \frac{\Delta t}{t_{ui}} \times 100\%.$$

For convenience, J is defined as the fractional jitter:

$$J = \frac{\Delta t}{t_{ui}}. \tag{4.49}$$

The jitter can be computed analytically if we consider that the line is driven (at the driver end) by the voltage waveforms shown in Figure 4.37. Signal A in

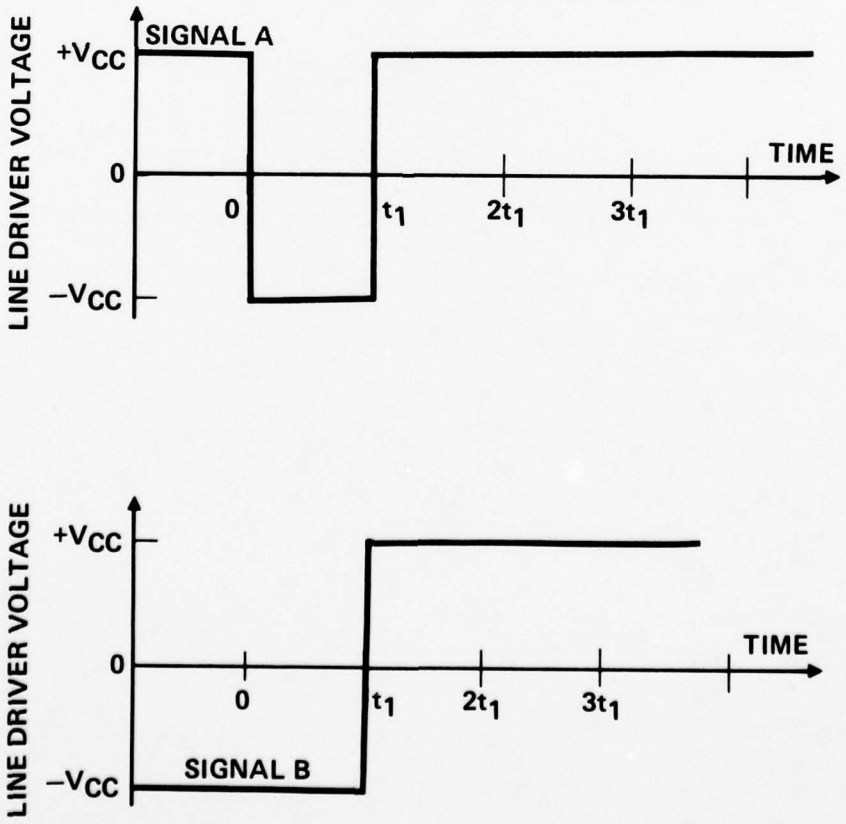


Figure 4.37. Voltage Waveforms Driving Transmission Line

Figure 4.37 is initially at a voltage level of $+V_{cc}$, switches to $-V_{cc}$ for a unit interval of time (the shortest pulse width expected in the system), then switches back to a voltage of $+V_{cc}$. Signal B is initially at a voltage level of $-V_{cc}$, then switches to a voltage level of $+V_{cc}$. The voltage responses of the two signals at the termination can be displayed superimposed on an oscilloscope, as shown in Figure 4.38. These two curves represent a portion of a complete binary eye

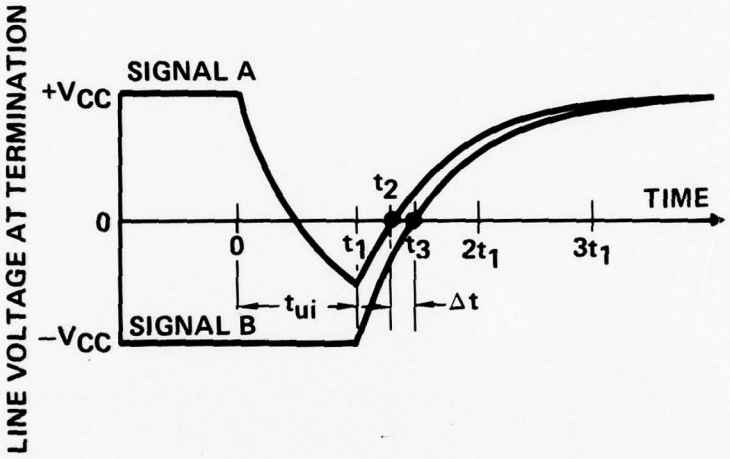


Figure 4.38. Signal Waveforms at End of Terminated Transmission Line

pattern. In calculating the response of the line to an applied signal, the line is assumed to be perfectly terminated and to charge exponentially. The three exponential waveforms V_0, V_1, and V_2 in Figure 4.38 can be represented by

$$V_0(t) = V_{cc}\, e^{-t/T} - V_{cc}(1 - e^{-t/T}) \qquad \text{for } 0 \le t \le t_1 \qquad (4.50)$$

$$V_1(t) = V_0(t_1)\, e^{\frac{-(t - t_1)}{T}} + V_{cc}(1 - e^{\frac{-(t - t_1)}{T}}), \qquad \text{for } t_1 \le t \qquad (4.51)$$

$$V_2(t) = -V_{cc}\, e^{\frac{-(t - t_1)}{T}} + V_{cc}(1 - e^{\frac{-(t - t_1)}{T}}), \qquad \text{for } t_1 \le t \qquad (4.52)$$

where T is the time constant of the line.

If we assume the receiver threshold is exactly zero, then receiver state changes will occur at times t_2 and t_3 in Figure 4.38. The difference, $\Delta t = t_3 - t_2$, is the widest timing variation possible in the received signal in relation to the

relative pulse positions in the transmitted pulse train (assuming the time delays through the driver and receiver for both logic states are symmetrical and have zero skew). The jitter is

$$J = \frac{t_3 - t_2}{t_1} \tag{4.53}$$

The value of t_1 is the width of a unit interval, so $t_1 = t_{ui}$, and the values of t_3 and t_2 can be calculated from Equations (4.50) - (4.52).

The effect of receiver threshold offsets is to modify the times t_2 and t_3 at which state changes occur. Receiver threshold changes can be induced when RF enters the input terminals of the line receivers. RF power inbalances at the two inputs can cause the threshold to become either positive or negative. In the general case, it is assumed that the receiver threshold can vary anywhere between the values $+V_{th}$ and $-V_{th}$. Since the RF fields are dynamic in general (the fields may change due to movement of the electronic system, due to movement of the source, as with a rotating antenna, or due to modulation of the source as in a pulsed radar), the receiver threshold must also be expected to change. In this analysis, the receiver threshold is conservatively allowed to vary instantaneously between any values between $+V_{th}$ and $-V_{th}$. Such threshold variations will induce additional jitter into the system which may make data transmission difficult.

Figure 4.39 is similar to Figure 4.38, but it shows the effect of variations in the threshold voltage. The widest possible timing variation is again $t_3 - t_2$, but the values of t_2 and t_3 (earliest and latest state switches) are modified by the variable threshold level. The jitter is given by Equation (4.53). Note that in order to obtain state switches at t_2 and t_3 as shown in Figure 4.39, the threshold voltage must change from a value of $-V_{th}$ to a value of $+V_{th}$ at some time t_4 such that $t_2 < t_4 < t_3$.

Solution of Equations (4.50) - (4.52) for t_2 and t_3 in Figure 4.39 gives

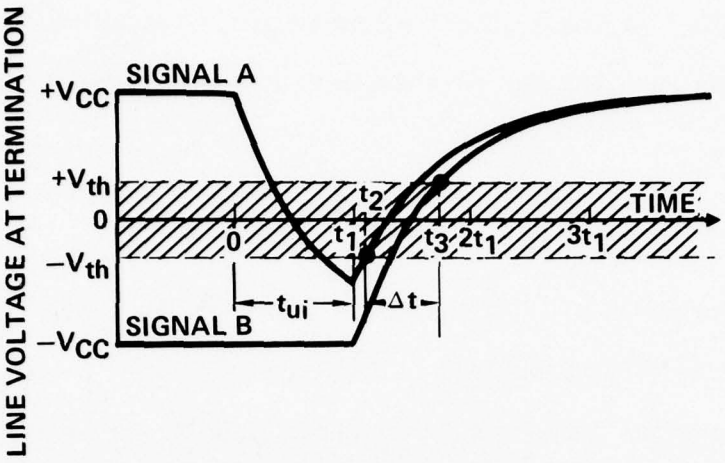


Figure 4.39. Signal Waveforms at End of Terminated Transmission Line With Varying Threshold Voltage

$$t_2 = \tau \ln 2 + \tau \ln[\exp(t_{ui}/\tau) - 1] - \tau \ln(1 + V_{th}/V_{cc})$$

$$t_3 = t_{ui} + \tau \ln 2 - \tau \ln(1 - V_{th}/V_{cc}),$$

which yields the following transcendental equation for J:

$$J = 1 - (\tau/t_{ui}) \ln[\exp(t_{ui}/\tau) - 1] + (\tau/t_{ui}) \ln[(1 + V_{th}/V_{cc})/(1 - V_{th}/V_{cc})]. \quad (4.54)$$

The time constant of the line τ can be expressed in terms of the time delay of the line in seconds per foot (t_d) and the line length (X):

$$\tau = X\, t_d/4.4. \quad (4.55)$$

Equations (4.54) and (4.55) were solved to obtain the graphs shown in Figures 4.40 and 4.41. Figure 4.40 shows the percent jitter as a function of line length, and data rate (data rate = t_{ui}^{-1}) when no threshold offsets occur. Figure 4.41(a)-(c) show the percent jitter when threshold offsets of $\pm 0.1\ V_{cc}$, $\pm 0.2\ V_{cc}$, and $\pm 0.4\ V_{cc}$ are possible. These graphs were made assuming t_d = 1.7 nsec/ft, which is a typical value for a twisted pair line. Comparison of the graphs in Figure 4.41 with Figure 4.40 shows that the jitter may increase significantly if threshold offsets occur. For example, with no threshold offset, a data rate of 12M bits/second, and a line length 100 feet, the percent jitter is given by Figure 4.40 as 5%. However, with a threshold offset of $\pm 0.2\ V_{cc}$, Figure 4.41(b) gives the jitter as 25%, a significant increase. Reference [13] recommends that

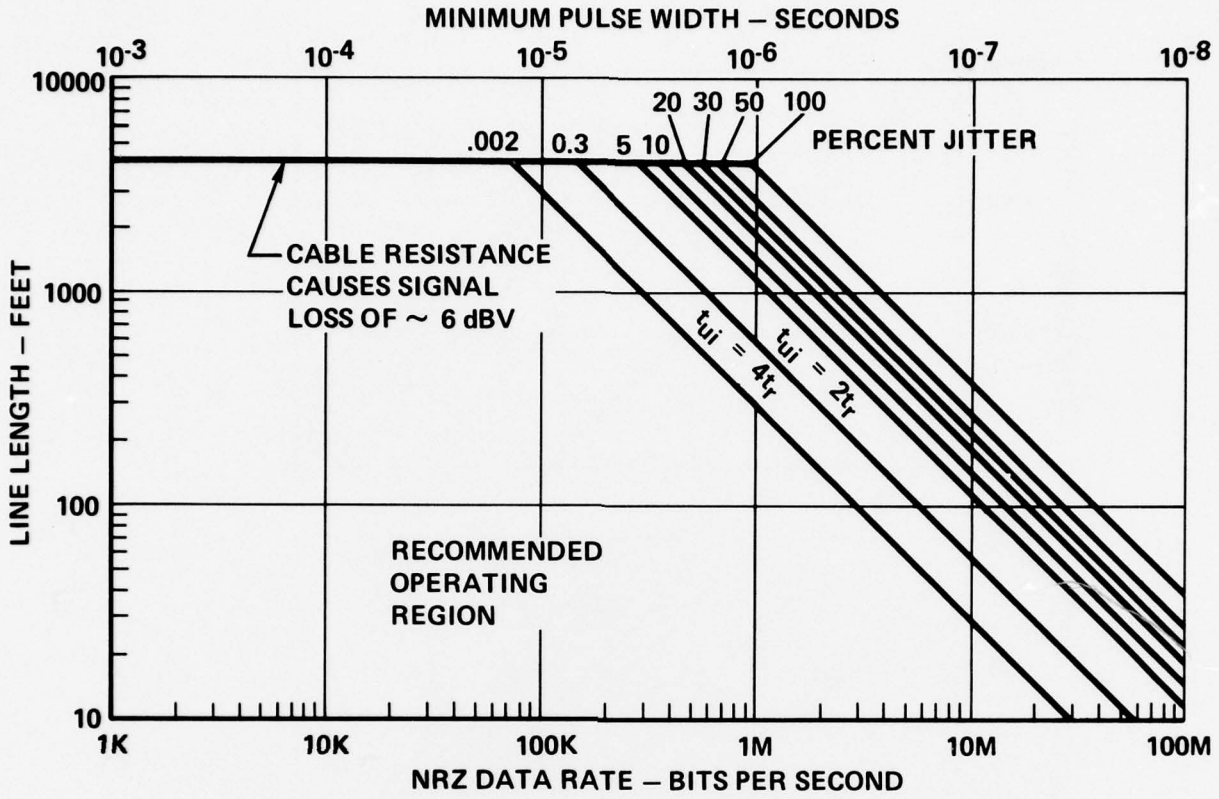
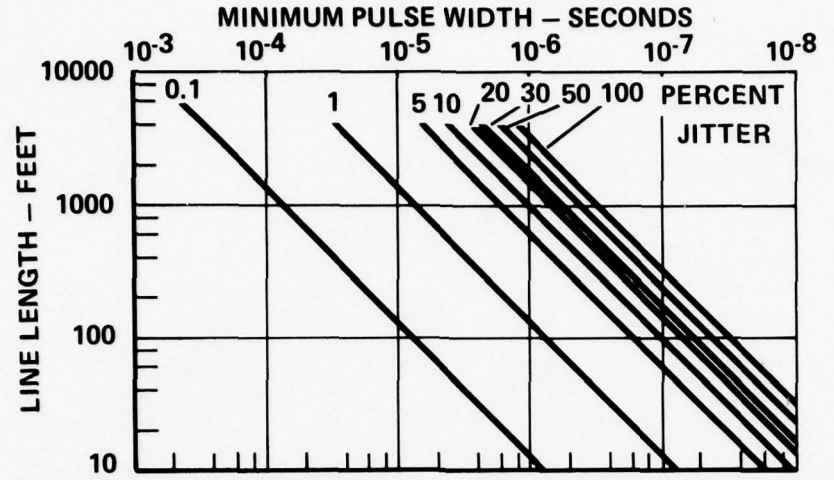


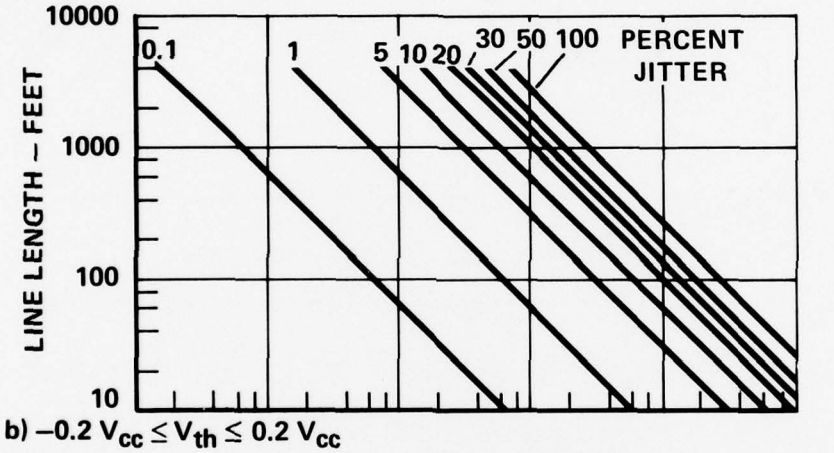
Figure 4.40. Signal Quality as a Function of Line Length and Data Rate

systems be operated with jitters less than 0.01% for reliable operation. Data with jitters greater than 100% are probably not recoverable.

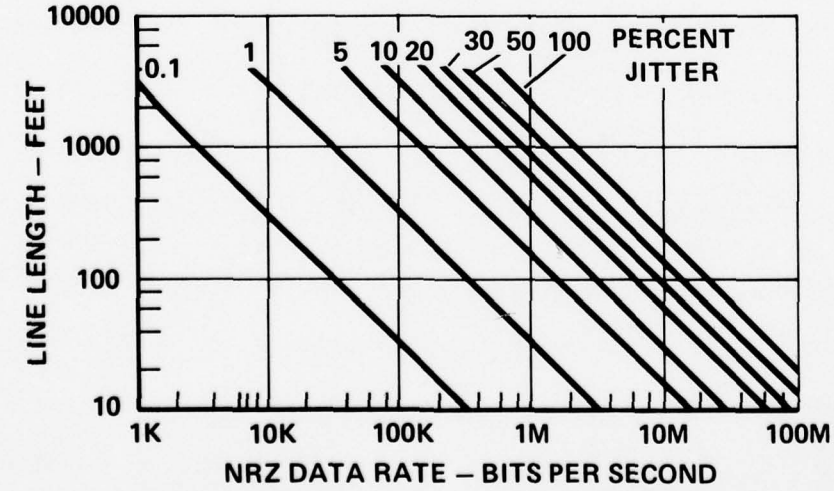
Information on threshold offsets versus RF power level has been measured experimentally. Figure 3.7 in this report shows worst case susceptibilities of five types of line receivers in terms of the threshold voltage offset. This graph can be used in conjunction with the graphs in Figure 4.41 to estimate the signal quality in terms of RF power and frequency. The important point for circuit and system designers is that when systems using line drivers and receivers and long transmission lines are required to operate in harsh electromagnetic environments, data transmission rates may have to be slowed in order to ensure reliable data communications.



a) $-0.1\ V_{cc} \leq V_{th} \leq 0.1\ V_{cc}$



b) $-0.2\ V_{cc} \leq V_{th} \leq 0.2\ V_{cc}$



c) $-0.4\ V_{cc} \leq V_{th} \leq 0.4\ V_{cc}$

Figure 4.41. Signal Quality as a Function of Line Length and Data Rate Including Effects of Threshold Voltage Offsets

CHAPTER 5

ELECTROMAGNETIC SUSCEPTIBILITY SEMINARS

Three Electromagnetic Susceptibility Seminars have been held during Phase III of the contract, the last two of which were held during this increment. The second Electromagnetic Susceptibility Seminar was held 19-20 October 1977 and had 83 attendees, while the third was held 25-26 October 1978 and had 46 attendees. All three seminars were held at the McDonnell Douglas Headquarters Building in St. Louis, and were jointly sponsored by the Naval Surface Weapons Center/ Dahlgren Laboratory and McDonnell Douglas Astronautics Company-St. Louis.

Although the first seminar was concerned mainly with integrated circuit susceptibility, the later seminars also included information on coupling and shielding, hardening design, system susceptibility and testing (including shielding effectiveness testing, laboratory EMV testing and full scale testing).

Included in the first two seminars were discussion sessions where valuable feedback was obtained on the Integrated Circuit Electromagnetic Susceptibility Handbook. Discussions centered around such topics as coupling approaches, shielding within electronic systems, RF impedances of integrated circuits, the RF susceptibilities of devices and technologies that were not specifically covered in the handbook, including microprocessors, low-power Schottky TTL devices, NMOS, etc., and the evaluation of interference when more than one interference source is present. Wherever possible, the comments that were received in these discussions were incorporated into the final version of the IC Handbook.

At the final seminar a special session was devoted to use of the IC Handbook, and included specific examples of determination of pickup levels, susceptibility levels for specific equipment, and shielding levels required to make the equipment satisfy customer specifications.

Based on our experience with these seminars, it appears that the ICES Handbook has been well received by the EMC community and is currently being used for a number of EMC related activities. Comments on the handbook have, in general, been favorable, and most users that have been in contact with MDAC consider it a valuable reference.

CHAPTER 6

CONCLUSIONS AND RECOMMENDATIONS

This report is the final output of the Integrated Circuit Electromagnetic Susceptibility Investigation conducted by MDAC. The program has been successful in characterizing, through both measurements and analytical approaches, the electromagnetic susceptibility properties of integrated circuits. The major output of this investigation was the ICES Handbook, which was published 1 August 1978. It summarizes the susceptibility information gleaned during this investigation in a form which can be readily applied to a variety of EMC design and analysis activities.

While integrated circuit technology may change rapidly in the coming years, and increasingly complex circuits may appear, the basic information contained in the ICES Handbook is expected to remain an accurate estimate of the susceptibilities of future integrated circuits. The reason for this is that the present interference mechanism, rectification, is not expected to change with advances in circuit complexity or technology. The handbook is expected to remain a valuable reference for many years to come. Based on verbal feedback and on the seminar attendance, the ICES Handbook has been favorably received, and is currently being used by the EMC community.

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This Section provides a list of the documents used as sources of information in preparation of this report. Reports referenced with a number of the form NXX-XXXXX are available through:

National Technical Information Service
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This report summarizes progress made in investigations into the RF susceptibility of integrated circuits (ICs). This report covers the work performed during the third of three increments. Included is a description of the revisions which were incorporated into the Integrated Circuit Electromagnetic Susceptibility Handbook (Report MDC E1929 dated 1 August 1978) which summarized all of the information obtained during the entire program in a handbook format for use by designers and EMC engineers. Results of tests of the susceptibilities of integrated circuits performed during this increment

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are described. Models of rectification in PN junctions developed during this increment are described. Simulations of interference effects in TTL NAND gates and 741 OP AMPs are included using computer-aided circuit analysis techniques and a modified Ebers-Moll transistor model which includes interference effects. Jitter effects due to RF interference in data transmission systems are discussed. This report includes a brief description of two Electromagnetic Susceptibility Seminars which were held during this increment.

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